

**Walkthrough 1
Transient Simulation of single and
4 inverter schematics**

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1 Introduction

This document is intended to replace the Spice Design Assignment for the AMI 4233 layout. Following this assignment within the Cadence design environment using the AMS 0.35um technology kit you will create and simulate MOS inverters.

Compared to the original walkthrough the change are:

Table 1:

Change	Original	Update
Design Kit	Mietec 2um	AMS 0.35
Simulator	cdsSpice	Spectre
Environment	Unix Direct	Linux Transport
IC Design	1999-2000	4.5/4.6

2 Conventions used in this document

The following are conventions that will be used in this document.

- Where user input is required it will be delineated with "<>".
- Where a special function key such as escape, control or return/enter is indicated in a command it will also be enclosed in "<>" brackets. For example "<RETURN>".
- Please be aware of spaces in words and commands. Like Windows and common English UNIX and Linux require spaces between commands.
- Unix and Linux commands are lower case unless stated. Unix and Linux are case sensitive.
- Operations involving the mouse will use the left hand mouse button unless otherwise stated.
- Options selected from sub menus will be indicated in the following manner

Main Menu Item -> Sub menu Item -> Sub Menu Item

- e.g. File -> New -> Library

2.1 Entering Parameters for commands

Unlike windows most UNIX/Linux parameters are delineated by a "<SPACE>". For example

- `grep -i fred *.v`

3 Accessing and Configuring the Design Environment

3.1 Opening a Terminal Window on the Linux Platform

Linux is, unsurprisingly, very similar to UNIX. It has become the defacto “technical” platform replacing or supersceding UNIX systems. The environment of the Linux platform has been configured to be as similar to the UNIX environment as feasible.

There are two ways to open up a terminal window in Linux

1. Move the mouse cursor onto the background of the Linux display and use the right hand mouse button to display the context sensitive menu. Select the Terminal option from this menu.

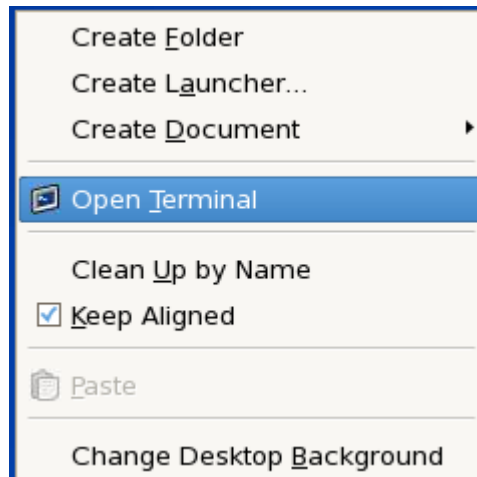


Fig: Background Context Sensitive Menu

2. Use the Application -> Accessories -> Terminal menu option on main menu.

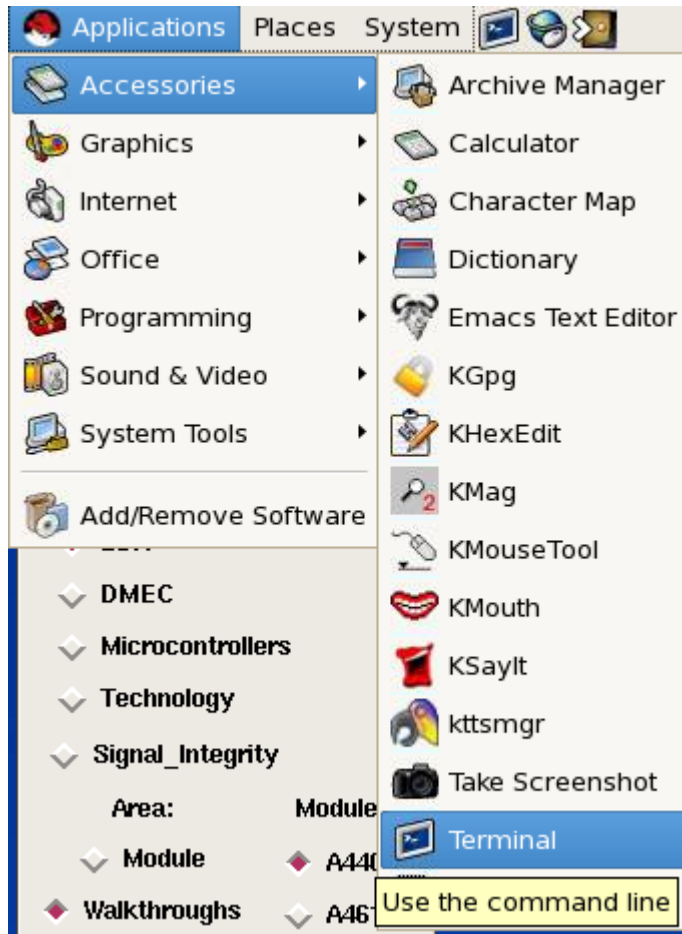


Fig: Linux Top Level Terminal Menu

4 Creating a Design Environment

Students using the AMI design system are provided with a Transport menu that facilitates easy access to appropriate design directories and associated applications software.

Accessing and Configuring the design environment is achieved using the “transport” tool. Students should start a UNIX terminal window and invoke the transport tool by typing the command:

- transport & <RETURN>

The *Transport* form should appear as shown below.

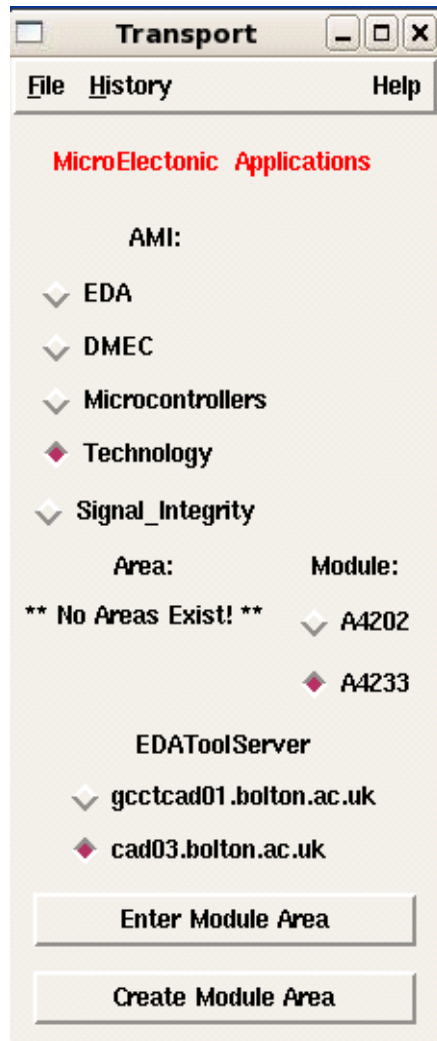


Fig: Transport Menu with no module areas created for A4233

The menu enables a module design area to be created and then entered by specifying the module being studied. Modules are classified by type and function.

4.1 Using the Transport Form

Click on the **Technology** button to display a list of modules within that classification.

- Select the module A4233

If you are using the transport tool for the first time for this module there will be no design areas present and the "Area" field will be blank. In this case you will need to create the default structure by using the "Create Module Area" button.

- Click on the **Create Module Area** button to the design areas.

Transient Simulation of single and 4 inverter schematics

The form should now resemble the one shown

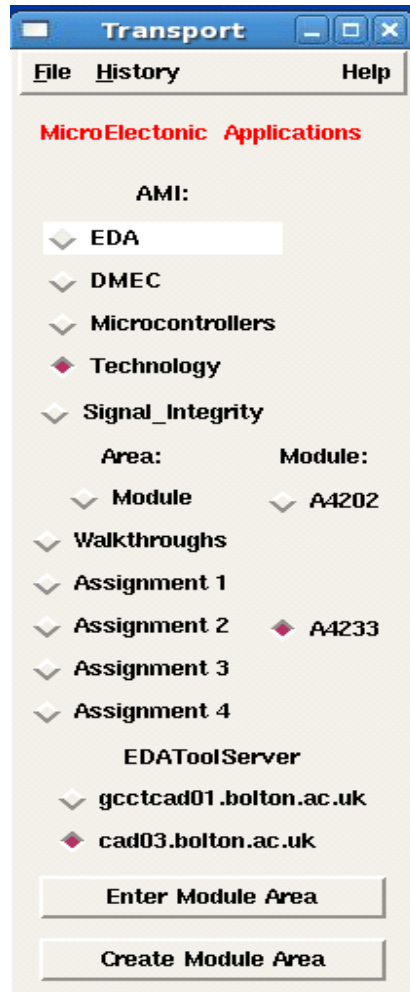


Fig: Transport form with A4233 area created

This may take a few seconds. Once this has run successfully the “Area” field will be populated. As shown in the figure “Transport Menu with module areas specified”.

Now select the Walkthroughs area. Only the *Walkthroughs* area will be used for this exercise.

- Click on the **Walkthroughs** button

The *Transport* menu should now be as shown below.

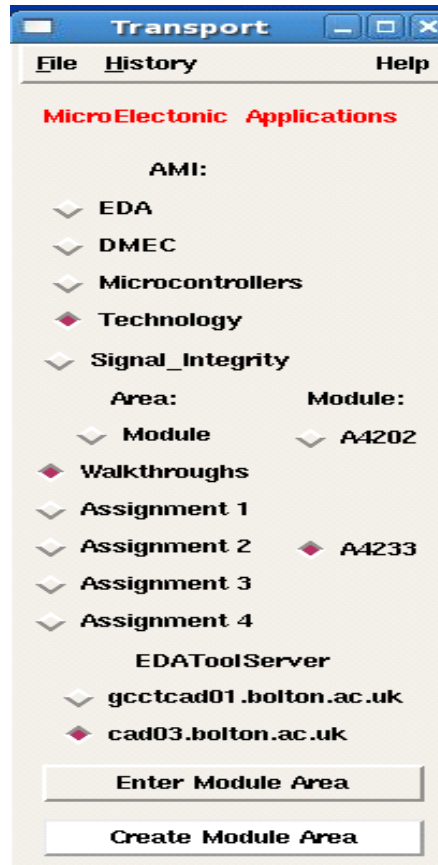


Fig: Transport Menu with module areas created and Walkthrough selected

Now click on the **Enter Module Area** button to open up a configured UNIX terminal window. All subsequent commands will be typed in this window. This window will be in the correct location, in this case the “Walkthrough” area. For the 4233 module this will be physically located at “~/AMI/A4233/Walkthroughs”. This area is also configured to allow you to run all the relevant tools required for the module.

5 Starting Cadence and the AMS 0.35um Design Kit

In the configured 4233 terminal window you can start the design kit using the UNIX command:

- **amiselect fb <RETURN>**

After a short delay the CADENCE Command Interpreter Window (CIW) as shown below will appear at the bottom of the screen. The window provides a tool bar for the top level menu commands and a display window for status information.

If this is the first time you have started the tools you will be presented with the form below to allow

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you to select the required process. The process requires is the C35B43. Select this and OK the form. On occasions this form can be obscured by other windows. If the Cadence tools freeze at the start Iconise windows and look for this form. This should only occur the first time you start the tools in a new directory.

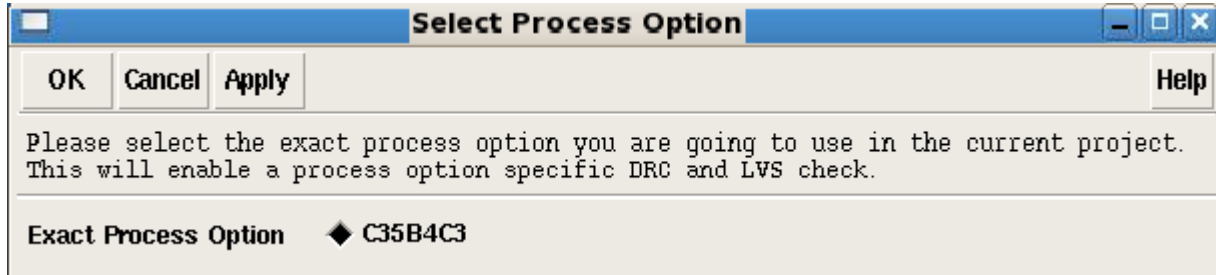


Fig: Select Process Option form

The other tools routinely displayed are the CIW and Library browser (not to be confused with the instance browser) tools.

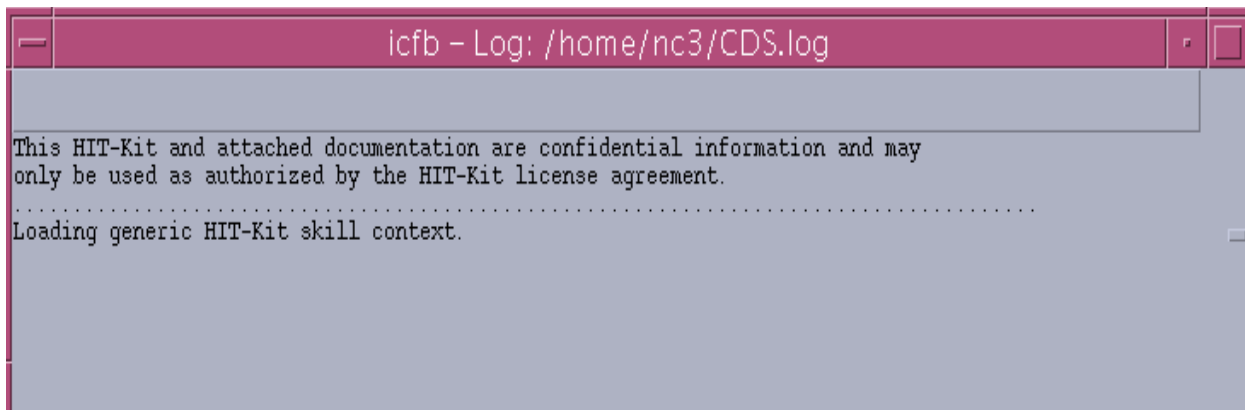


Fig: The CADENCE Command Interpreter Window (CIW)

The Cadence *Library Manager* as shown below will also be displayed.

Transient Simulation of single and 4 inverter schematics

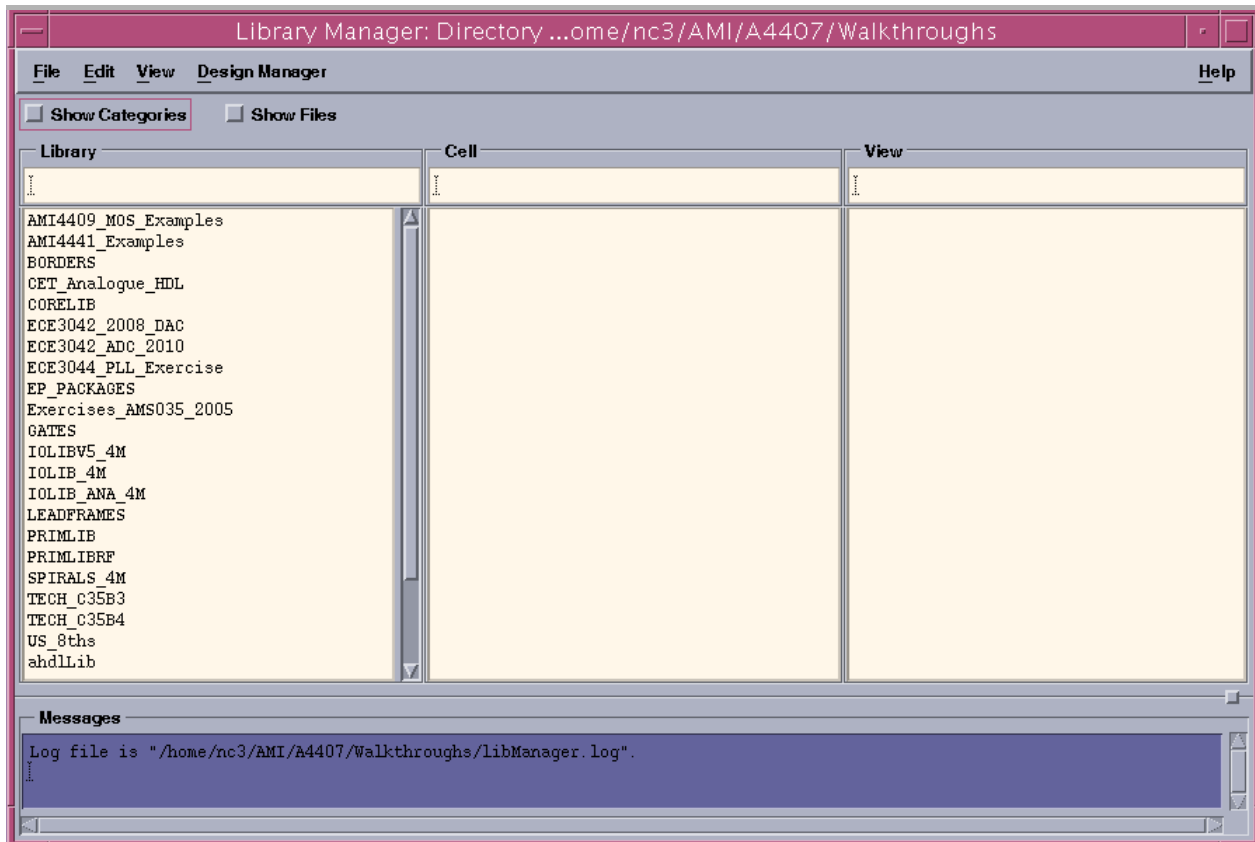


Fig: Library Manager

The *Library Manager* enables design libraries, cells and cell views to be created, opened, copied and of course renamed/deleted etc.

6 The Single Inverter Schematic

The inverter exercises have already been pre-prepared for you.

Cell *cmosinv1* defines a single inverter, cell *cmosinv4* defines a quadruple inverter circuit, both of these are in the *Exercises_AMS035_2005* library.

We shall use the *File Manager* to select and display each circuit.

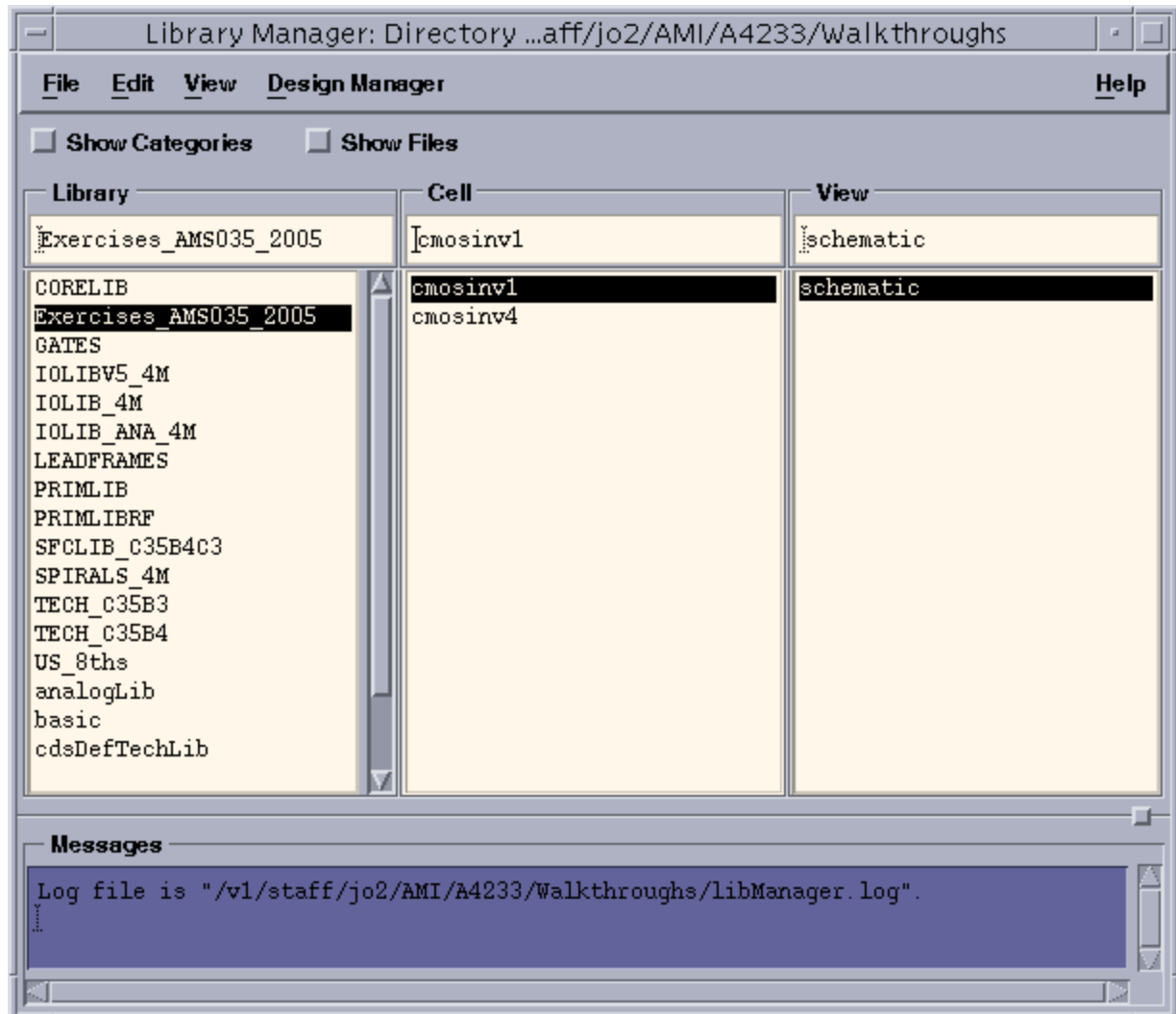
Locate and select by clicking on the following in the *File Manager* :-

- **Exercises_AMS035_2005** in the *Library* column,
- **cmosinv1** in the *Cell* column and
- **schematic** in the *View* column (if required)

The *File Manager* should now be as shown below.

Transient Simulation of single and 4 inverter schematics

Select **File - Open** from the *File Manager* toolbar to open the selected schematic (*cmosinv1*)
Since this file is write protected, the system will display a message to open for read only.
Select **Yes** to display the *Schematic Window* as shown below.



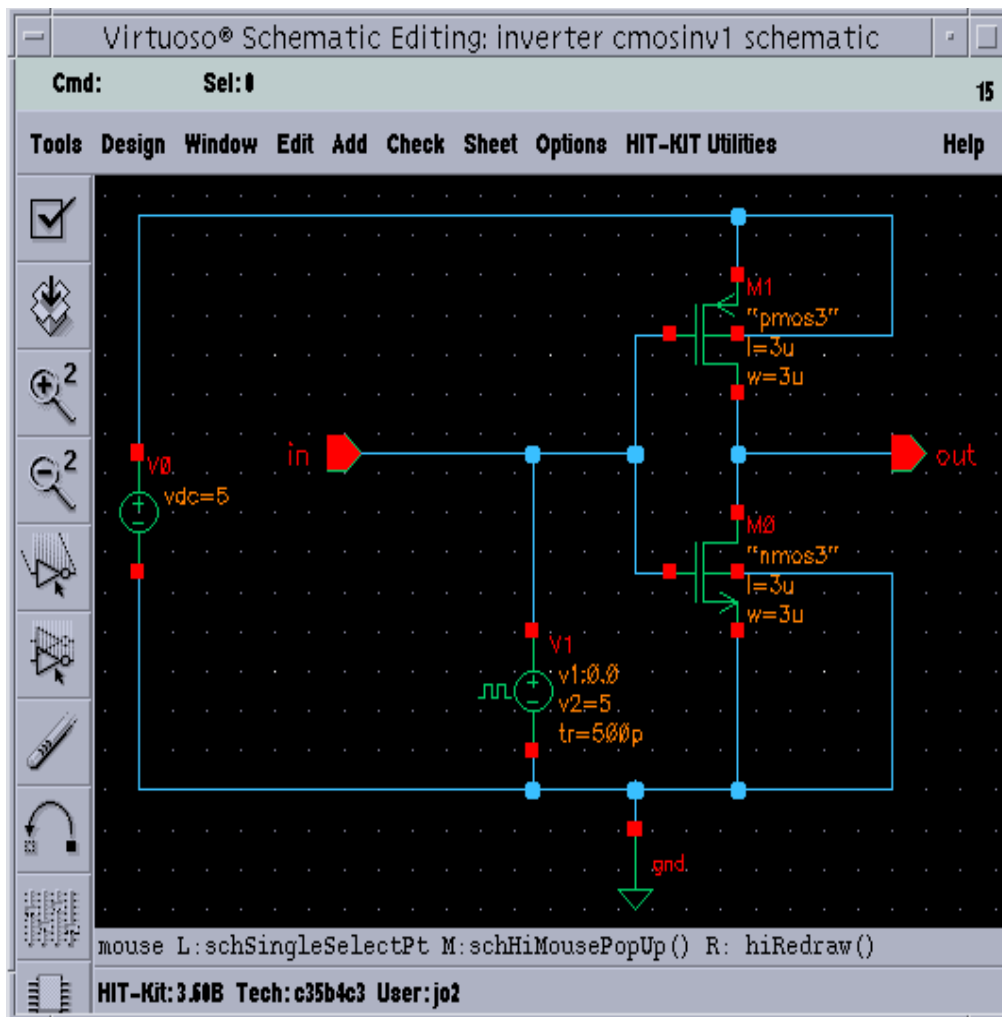


Fig: Single Inverter Test Schematic

At this point you may wish to minimise all other windows except the CIW to avoid the desktop becoming too cluttered (click on the dot icon at the top right of each window). Any minimised window can be restored by double clicking on its icon. You may also wish to maximise the *Schematic Window* (click on the square icon at the top right of the window). Linux does support multiple desktops for those familiar with this facility. However it would be sensible to avoid opening multiple copies of the Cadence tools to avoid file locking issues.

The schematic defines a simple CMOS inverter consisting of one PMOS and one NMOS transistor. The channel widths and lengths of both transistors are set to the minimum process dimensions (3 microns). The device will be operating under no load conditions from a 5 volt power supply. A pulsed voltage source of 4ns duration at the input will test the device in both of its operating conditions. The rise and fall times of this pulse have been set comparable to those of the device (0.5ns).

6.1 Setting up the Simulation

The simulation will be performed using the Spectre simulator.

Transient Simulation of single and 4 inverter schematics

This is located in the *Analog Design Environment* tool of Cadence.

Select **Tools - Analog Environment** from the schematic window menu. This will open the Analogue design

The Cadence *Analog Design Environment* form will appear as shown below with spectre selected as the simulator

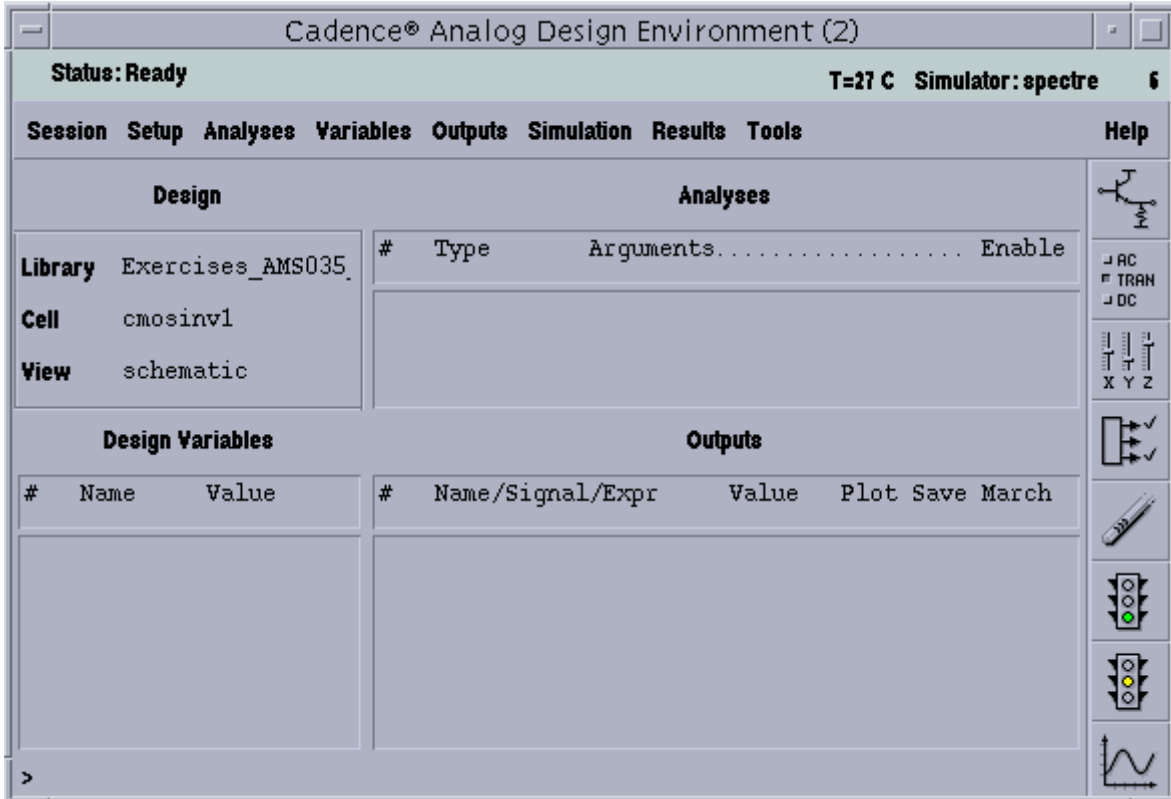


Fig: Analog Design Environment Form Initial format

Before the simulation can take place it will be necessary to set up the parameters for a transient analysis. A transient analysis plots a graph of a selected circuit voltage or current against time. The parameters define a length of time for which the simulation should run. Since the applied input pulse has a 1ns duration the simulation must proceed at least to the end of this pulse. A stop time of 3.5ns will be adequate.

Select **Analyse - Choose** [or the **AC/TRAN/DC** icon second down on the right] from the *Analog Design Environment* form to display the *Choosing Analyses* form.

Select the **tran** button from this form and enter a value of **12n** into the *Stop Time* box.

The form should now be as shown below :-

Transient Simulation of single and 4 inverter schematics

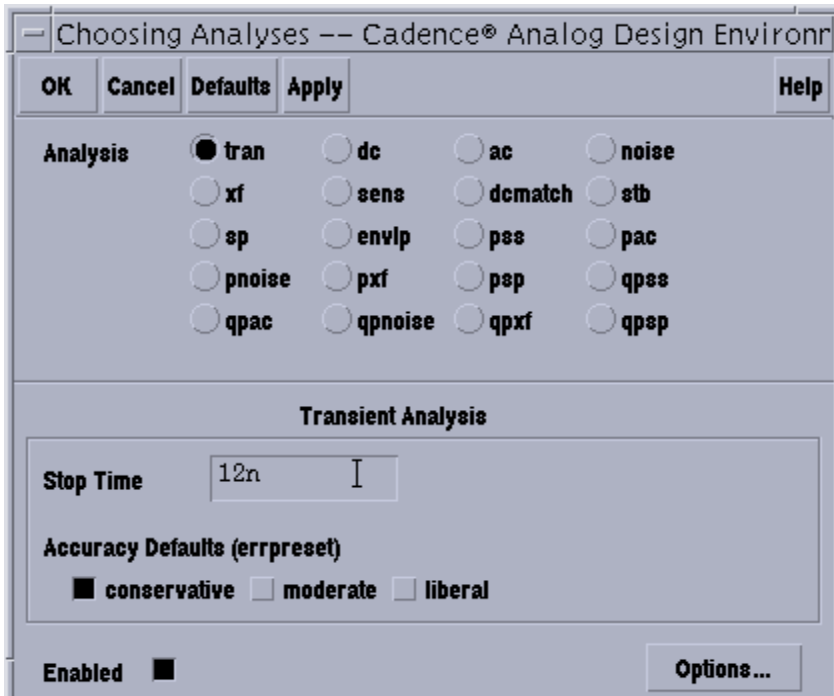


Fig: Choose Analysis Form with Transient Options

OK the form and check that the parameters have now been entered into the *Analyses* section of the *Analog Design Environment* form as shown below

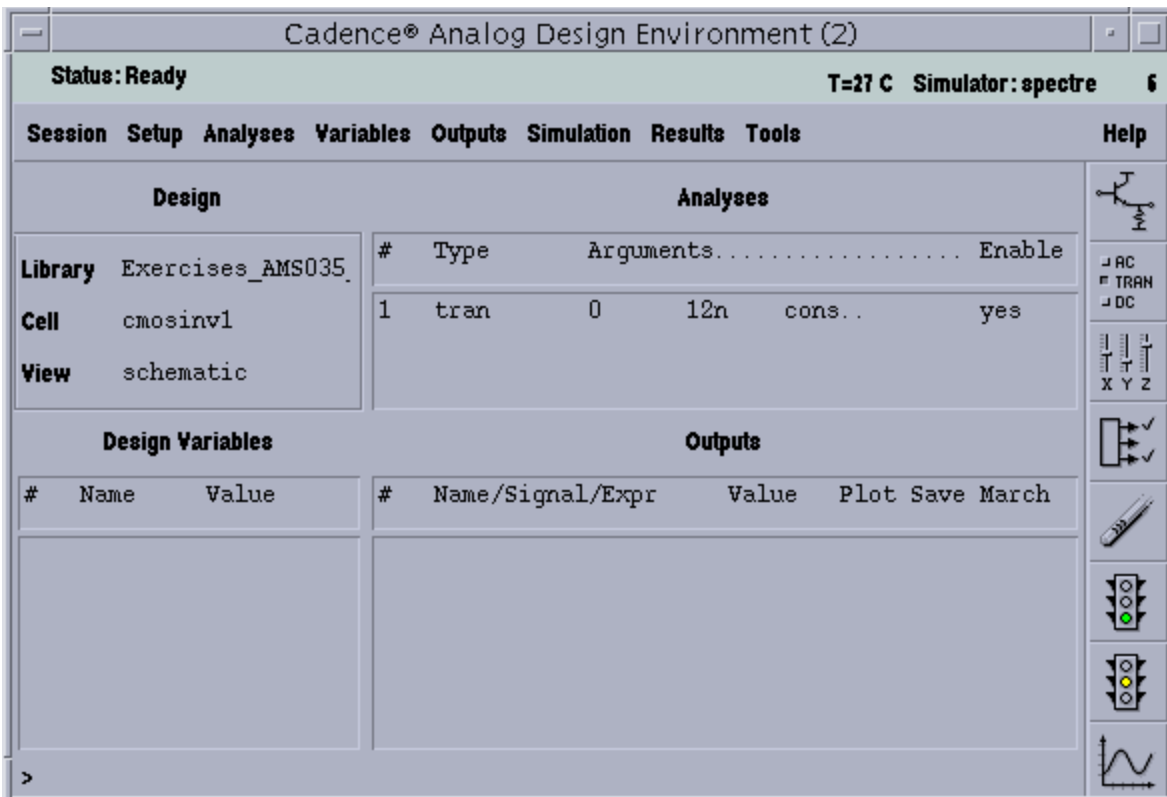


Fig: Analog Design Environment form with transient simulation shown

6.2 Running the Simulation

Select **Simulation - Run** [or the **green traffic light** icon] to run the simulation.

The first time a simulation is run the system will display a *Spectre Welcome* message.

Having read the message click the "**Do not show this text again**" button

This avoids repeated occurrences of the message.

Select **OK** on the message toolbar to run the simulation

During the simulation, status information and any possible error messages are displayed in the CIW.

You can maximise the window to see all of this information.

Check the messages to verify that the simulation has terminated successfully

At the end of the simulation, a window will open displaying the simulation log file.

The file contains useful information about the simulation run and error conditions should the simulation be unsuccessful. You may see warnings relating to the model parameters. These can be ignored.

Select **File -Close Window** to close the window.

6.3 Displaying the Simulation Results

Select **Results - Direct Plot - Transient Signal** from the *Analog Design Environment* form

An empty *Waveform Window* will be displayed with the schematic window eventually overlaid on top.

The *Schematic Window* now enables signals to be selected for display.

The input from the pulse generator and the circuit output will be displayed.

Click anywhere on the input wire or pin labeled **in**

A successful selection will highlight the wire in a new colour.

(Avoid clicking on the connecting dots, this will not register)

Click anywhere on the output wire or pin labeled **out**

Again observe that the wire highlights in a new colour.

The schematic should now be as shown:

Transient Simulation of single and 4 inverter schematics

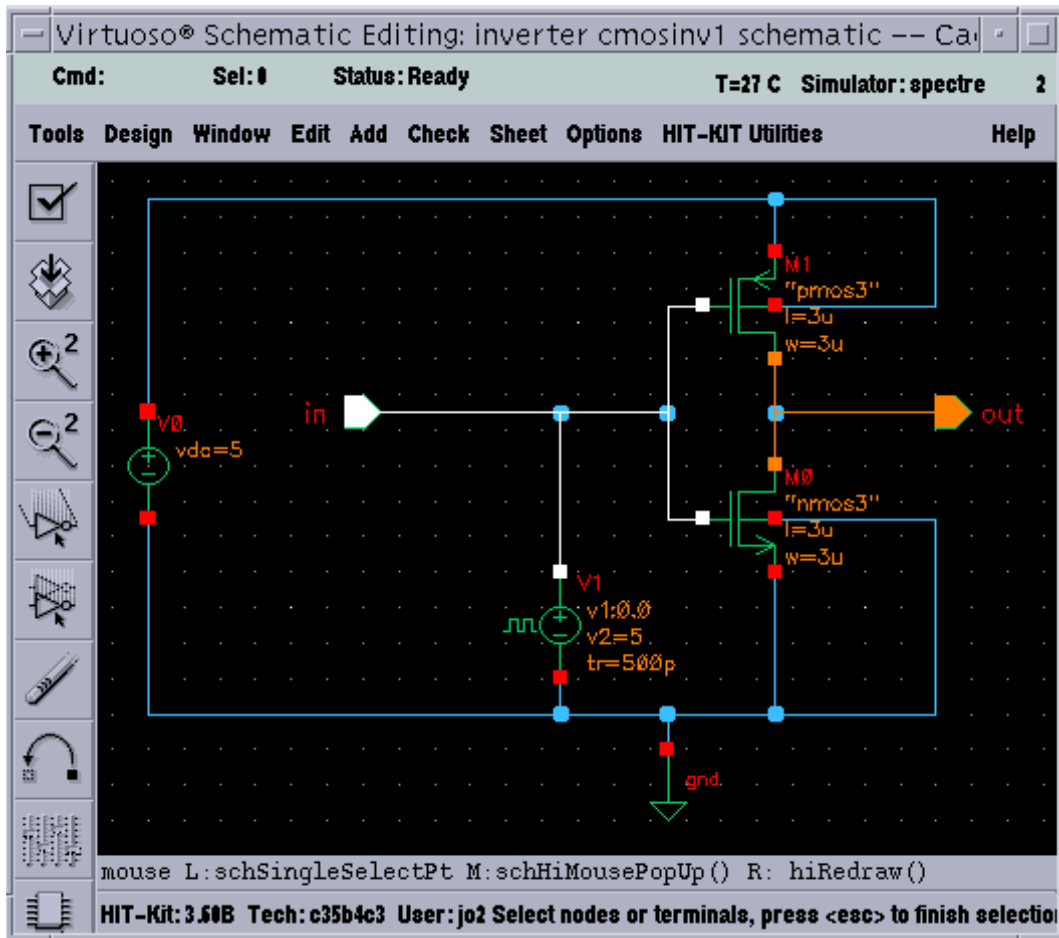
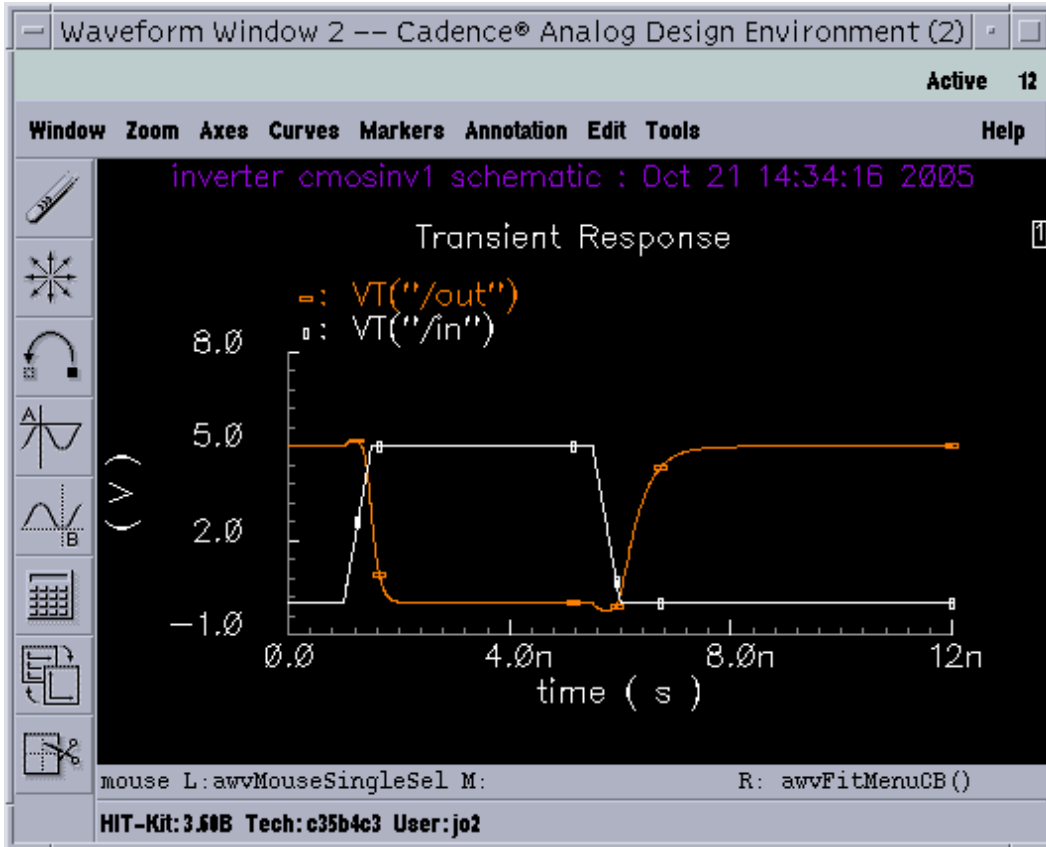


Fig: Schematic Showing Selected nets

Press the **Esc** key to terminate the selection process, whilst the mouse is in the schematic window!
The selected waveforms are now displayed in the *Waveform Window* as shown below.



Waveform Display Showing Rise/Fall of Input and Output Waveforms

The window can be enlarged to full size if desired by clicking on the square icon in the top right hand corner of the window or using the options under the **Zoom** menu.

The waveforms can be viewed more easily by splitting the display.

Select **Axes - To Strip** from the *Waveform Window* to produce the display shown below

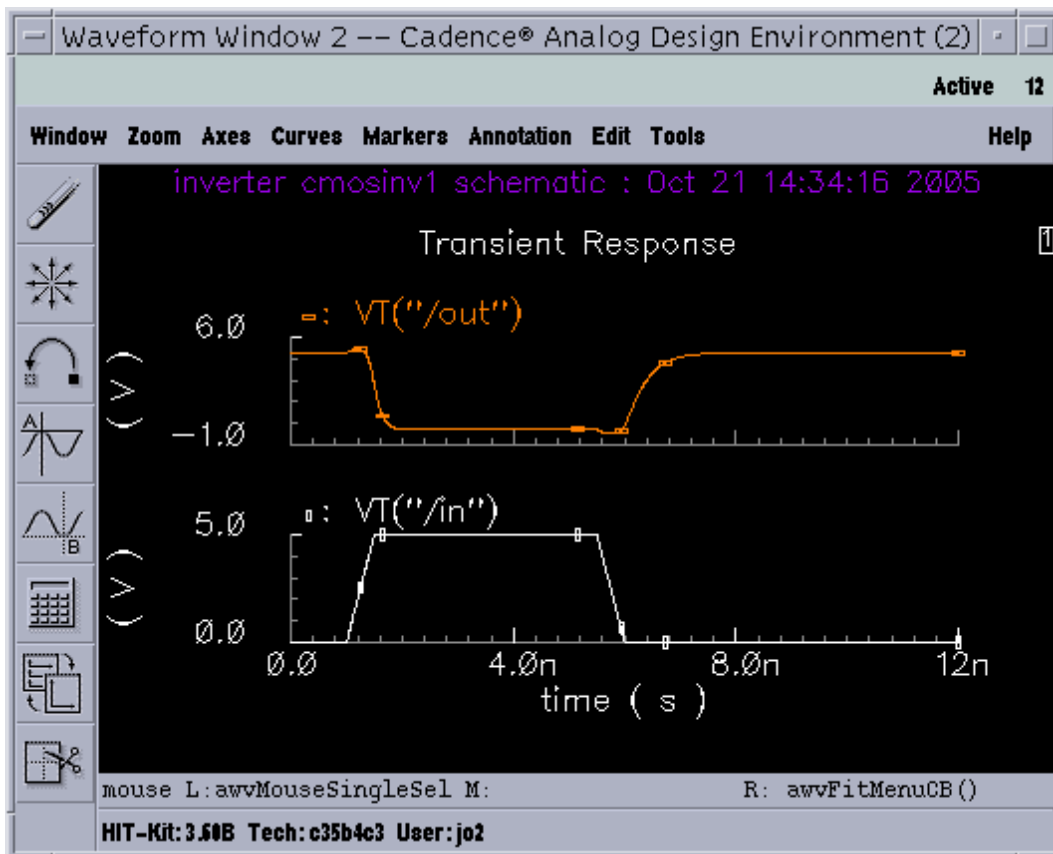


Fig: Waveform window with strips option selected

6.4 Measuring the Single Inverter Timings

The time taken for the output of a device to switch to its opposite logic state upon the application of an input signal is referred to as the *Propagation Delay*. For a single logic element, this propagation delay is defined by how fast the output can switch between states. The time taken to achieve this is known as the *Switching Time*. The switching time for a low to high transition of the output is referred to as the *Rise Time* whilst that for a high to low transition defines the *Fall Time*. When several devices are connected in series in a logic circuit these switching times become additive. Logic designers (and logic simulators) use the device switching times to calculate overall propagation delays for the circuit. Outputs rise and fall exponentially due to the charging and discharging of device capacitances. You can observe this on the simulated output waveform, particularly in relation to the rising edge. Since the time taken to reach a new steady voltage level can be lengthy, rise and fall times are conventionally measured between 10% and 90% of their voltage swing

To obtain accurate measurements for the output rise and fall times it will be necessary to isolate and enlarge the output waveform.

Select **Curves - Edit** from the *Waveform Window* to display the *Curves* form.

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The form enables waveforms to be selectively displayed.

We shall remove the input waveform from the display.

Select the input waveform **VT("/in")** in the *Curve Name* column so that it highlights.

Click the **off** button.

The form should now be as shown below with the waveform's *Display* column entry set to *off*.

Curve Name	Display
1 VT("/in")	off
2 VT("/out")	on

Fig: Waveform curves edit tool

OK the form and observe that only the output waveform is now displayed.

You may also wish to remove the plot points on the waveform (known as *ticks*) to obtain a smoother curve

Select **Curves - Options** from the *Waveform Window* to display the *Plot Style* form

Enter **0** into the *Number of Ticks* box as shown below,

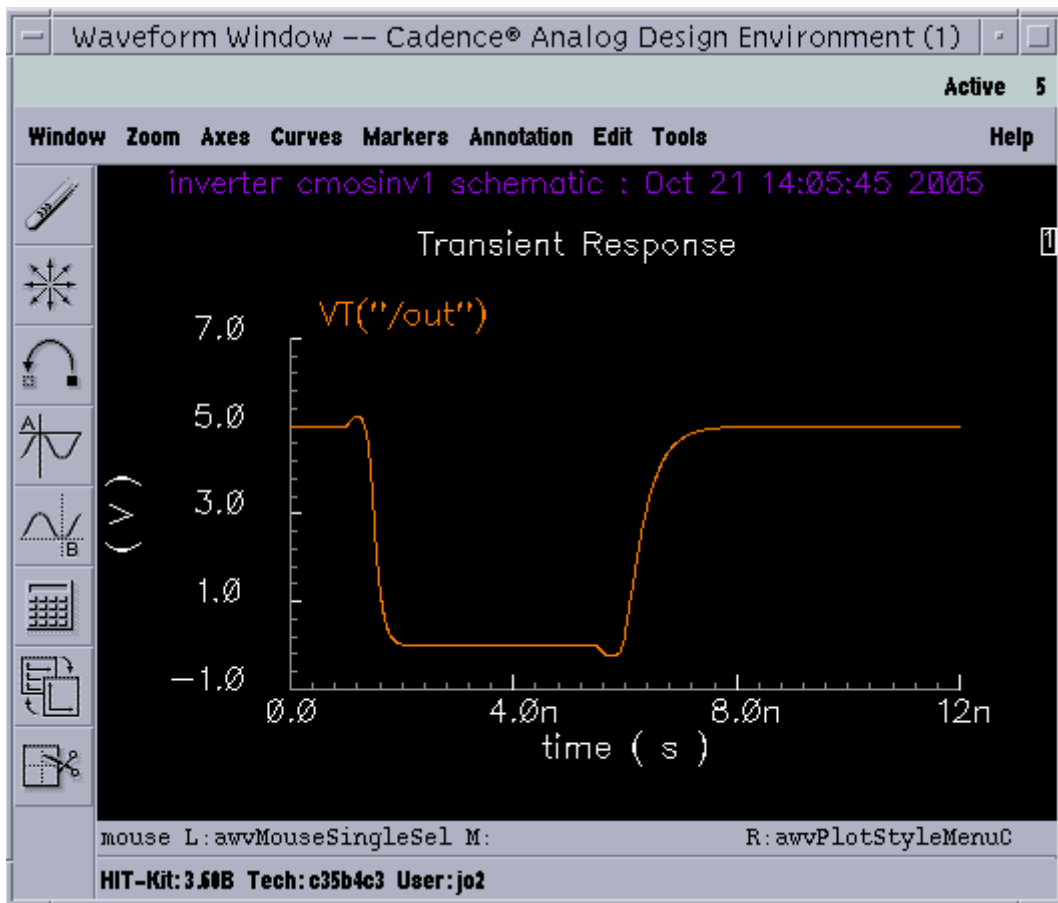
Plotting Style: Auto

Tick at Every Point:

Number of Ticks: 0

Fig: Plot Style Form

OK the form. The display should now be as shown below:



The zoom facility is used to enlarge the waveform.

The first area of interest is the waveform's falling edge

Select **Zoom -Zoom In** from the *Waveform Window*

Position the cursor at the top left of the zoom area (i.e. near the top of the falling edge of the waveform).

Press the left hand mouse button.

Drag the cursor to the bottom right of the zoom area (i.e. near the bottom of the falling edge of the waveform).

Press the left hand mouse button again.

The zoom function will now be activated and the display should be as shown below.

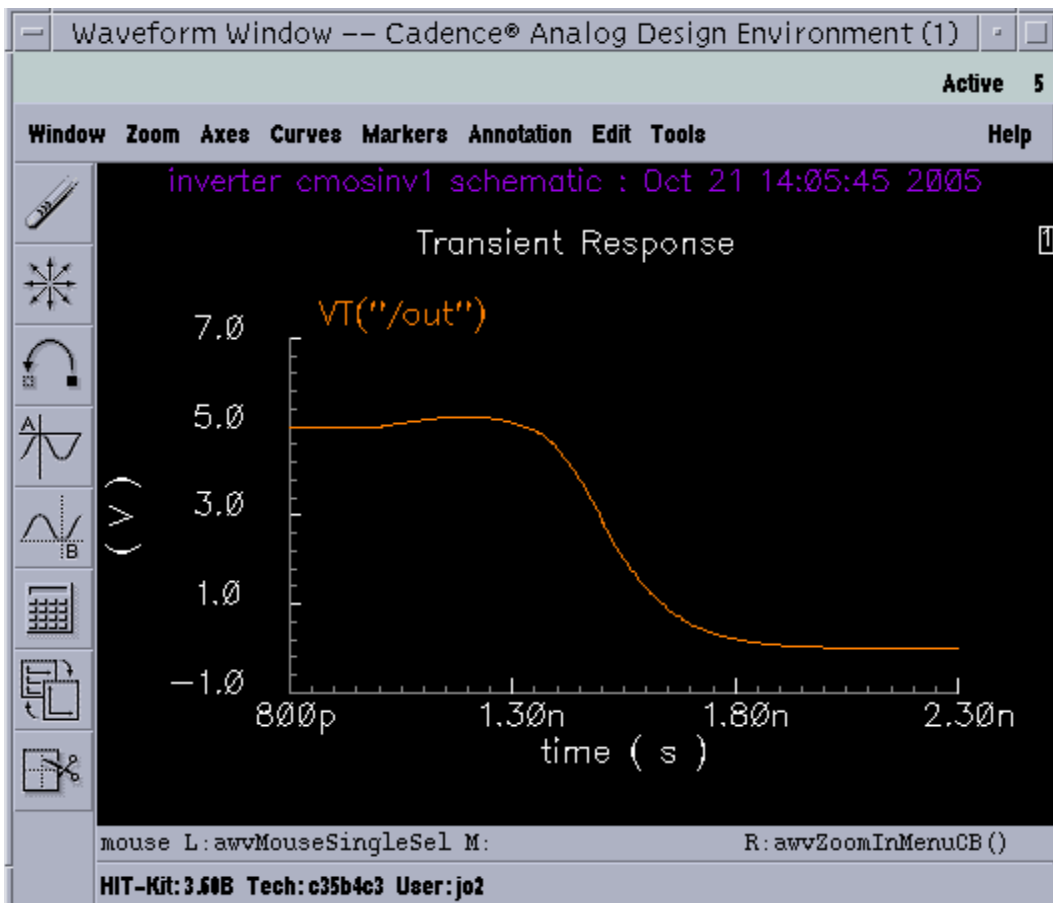


Fig: Zoomed in waveform display

The display can be returned to normal size at any time by selecting **Zoom - Fit**.

Crosshair Markers are useful for taking timing measurements from the waveform.

Select **Markers - Crosshair Marker A** from the *Waveform Window*.

Position marker A at the top of the falling edge at a voltage of 4.5 volts (90% marker).

The current location of the marker is displayed as an x/y co-ordinate at the bottom of the window.

Press the left hand mouse button to lock the marker

Select **Markers - Crosshair Marker B** from the *Waveform Window*.

Position marker B at the bottom of the falling edge at a voltage of 0.5 volts (10% marker).

Press the left hand mouse button to lock the marker

Should you wish to unlock the markers for re-positioning, simply re-select the **Markers** option.

The display should now be as shown below:

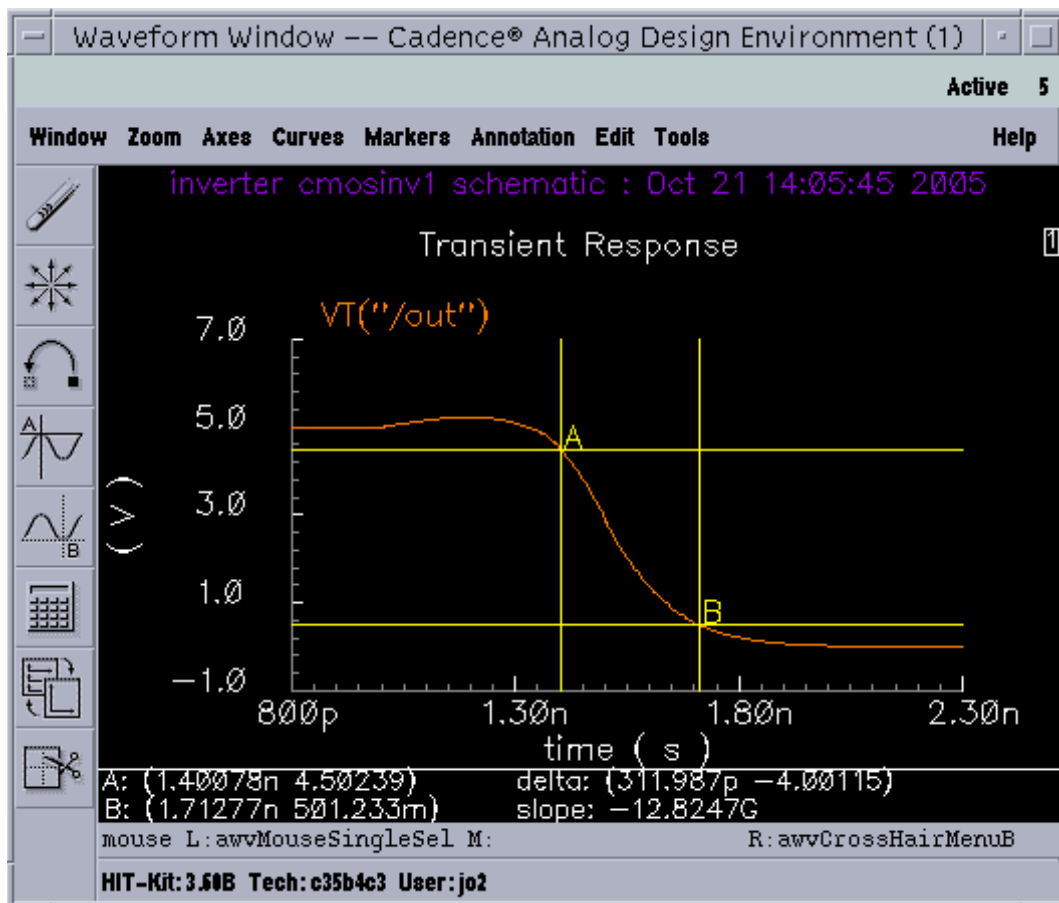


Fig: Waveform display showing A and B cursor and measurements

The delta reading at the bottom of the window indicates the time difference between markers. This is the fall time and will be of the order of 0.31ns .

Display the entire simulation again by selecting **Zoom - Fit**.

Repeat the above procedure for the rising edge of the waveform. This is the rise time and will be of the order of 0.80 ns.

The rise time is longer than the fall time because the PMOS and NMOS transistors have been defined on the schematic as having identical channel dimensions. Since the mobility of holes in the PMOS device is typically two to three times less than that of electrons in the NMOS device, the PMOS device will take proportionally longer to switch.

From the above timings we can therefore determine that the device propagation delays under no-load conditions are :-

For a low to high transition = **0.80ns**

For a high to low transition = **0.31ns**

Select **Window - Close** from the *Waveform Window* to close down the waveform window
Leave all other windows open

7 Simulating the Quadruple Inverter Circuit

The quadruple inverter circuit utilises four of the previous single inverter cells connected in series.

Delays inherent in the circuit will now be noticeably longer. In particular there will be :-

- a) Increased switching delays for each transistor caused by the additional input capacitance of its driven load.
- b) Increased overall propagation delay with 4 devices in series.

Both these effects will be observable by simulation.

Select **Design - Open** from the *Schematic Window* to display the *Open File* form.

Click on the cell name **cmosinv4** in the *Cell Names* list and check that it appears in the *Cell Name* box.

Click on **OK** and select **Yes** to open the file for read only.

The circuit is now displayed as shown below.

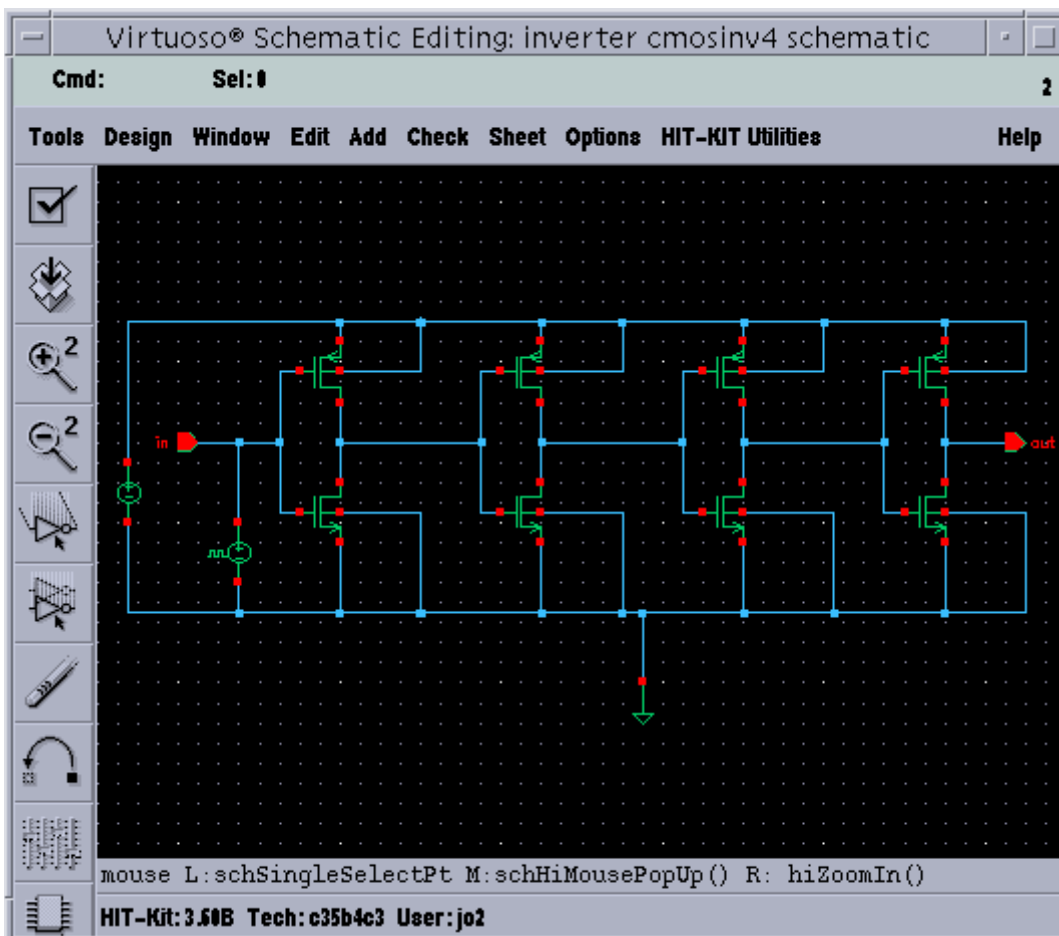


Fig: 4 Inverter Schematic

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Click in the Cadence *Analog Design Environment* form.

Select **Setup - Design** to display the *Choosing Design* form as shown below

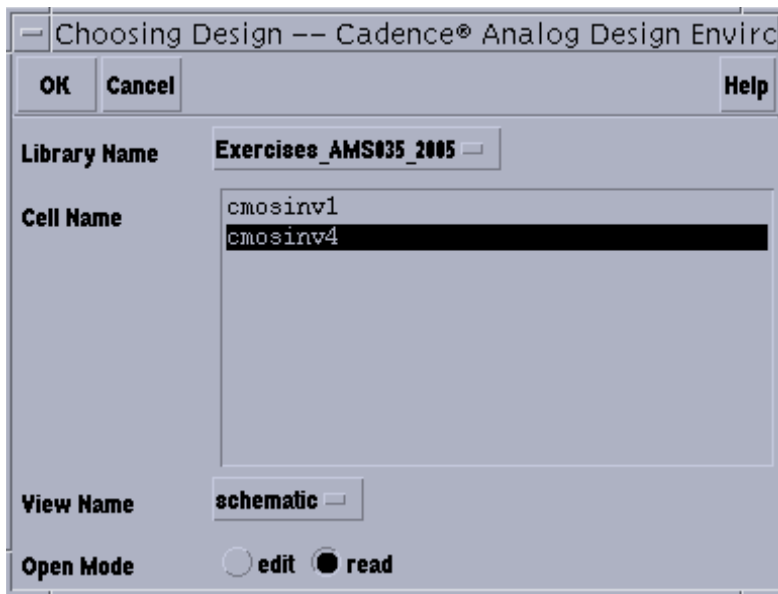


Fig: Choosing Design Form from Analogue Environment Tool

Select the **cmosinv4** cell and **OK** the form.

Select **No** in response to the query "*Do you want to save the current state?*"

This would normally save your simulation parameters but is not necessary for this exercise.

The design specified in *Analog Design Environment* form will now be reset to *cmosinv4*.

Follow the same procedure as established for the single inverter to simulate the circuit.

Use the same transient analysis parameters.

Select and display the waveform at the circuit input, the first, second and third inverter output wires and the final circuit output.

The display should be as shown below

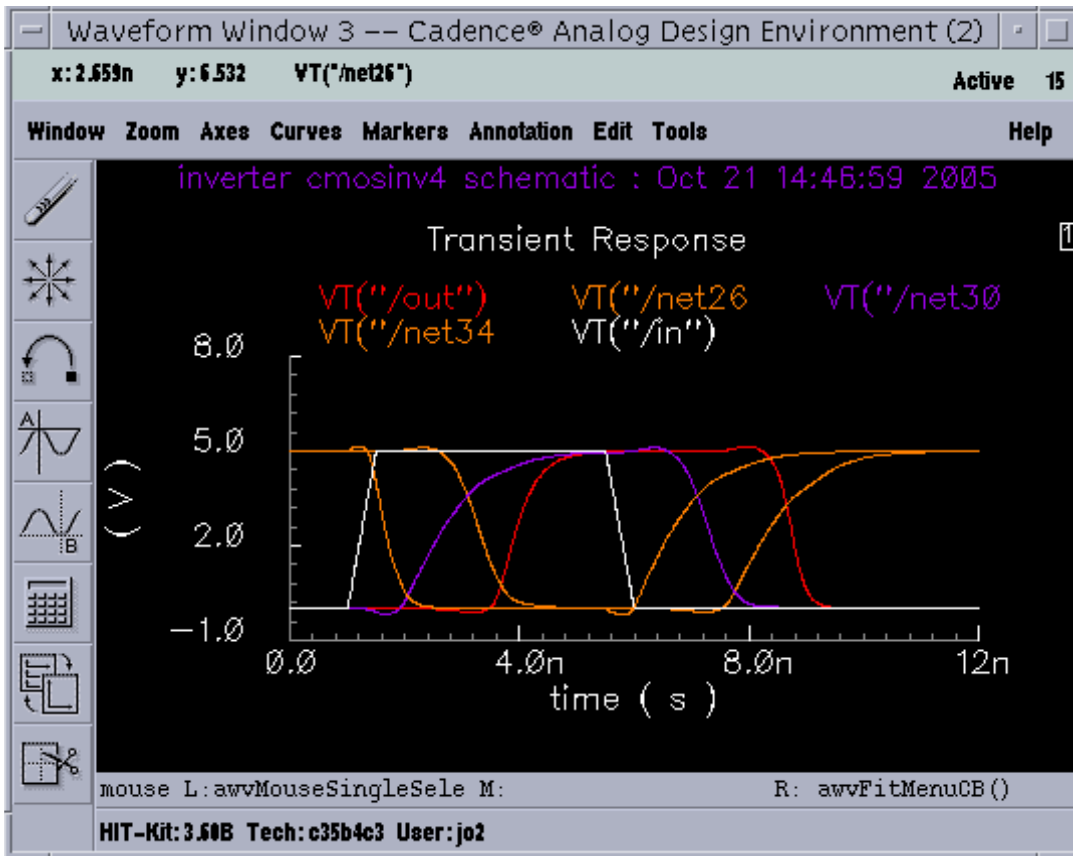


Fig: Waveform Window with Multiple nets selected

7.1 Measuring the Quadruple Inverter Timings

Temporarily remove all waveforms from the display (**Curves - Edit** option) except the output of the first inverter (net34).

Measure the new rise and fall times.

Verify that the fall time under loaded conditions has increased to the order of 0.57 ns

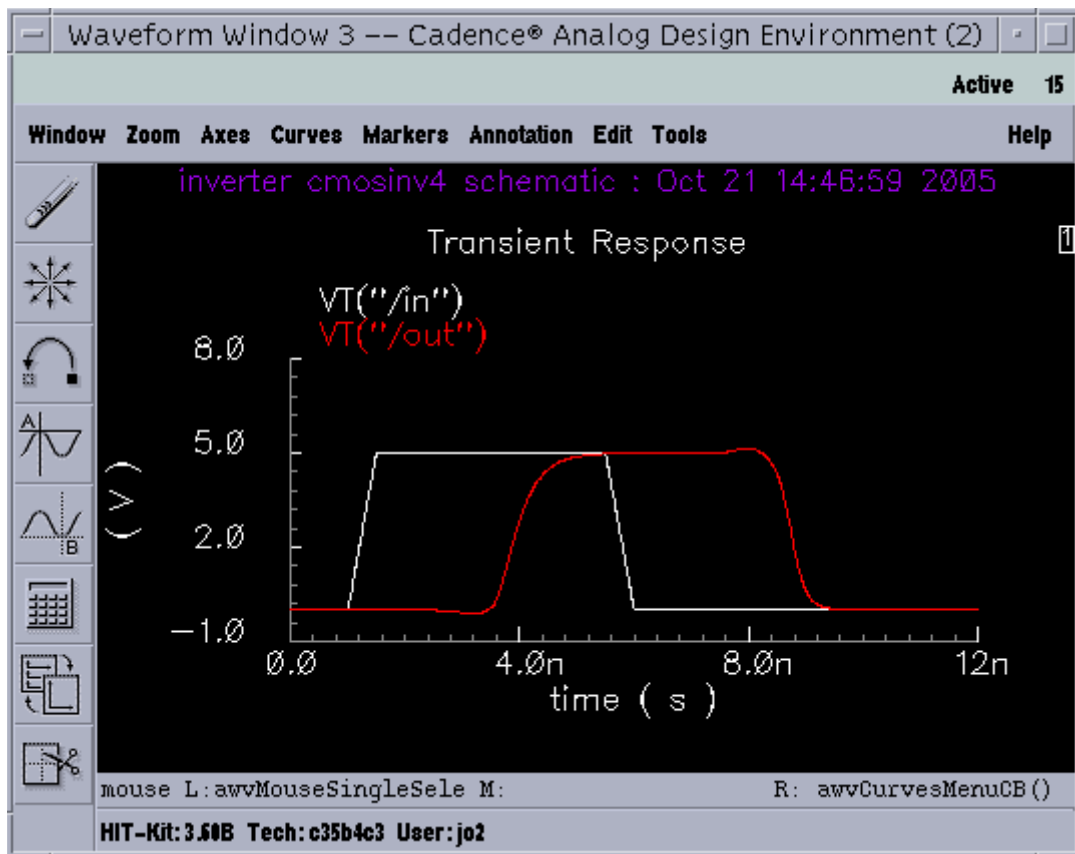
Verify that the rise time under loaded conditions has increased to the order of 1.79 ns

From the above timings we can therefore determine that the device propagation delays under loaded conditions are:-

For a low to high transition = **1.79ns**

For a high to low transition = **0.57ns**

Remove this waveform from the display and re-instate both the input and output waveforms as shown below.



Observe that the total propagation delay through the four inverters is considerably longer than that for the single inverter. Logic simulators calculate this delay by adding together the loaded propagation delays for each of the logic elements.

From the timings previously obtained, the delays for this circuit would be :-

For a low to high transition = $0.57\text{ns} + 1.79\text{ns} + 0.57\text{ns} + 0.8\text{ns} = \mathbf{3.73\text{ ns}}$

For a high to low transition = $1.79\text{ns} + 0.57\text{ns} + 1.79\text{ns} + 0.31\text{ns} = \mathbf{4.46\text{ ns}}$

(Note: the final inverter has no load)

The above figures will be approximate. In actual fact the circuit dynamics are quite complex. Devices will begin to switch when their input signal reaches the threshold voltage. Using the full rise and fall times in calculations implies a switch near to full value. Rise and fall times on device outputs are also dependent on the rise and fall times of their inputs. The analysis assumed a constant input rise / fall time of 0.5ns which is only true for the first inverter in the circuit. Both these effects can be observed on the previous waveform display where all device inputs and outputs are selected.

8 Leaving CADENCE

It is good practice to exit applications software in an orderly fashion and leave a clean desktop

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Select **Window - Close** in the *Waveform Window* to close the window.

Select **Window - Close** in the *Schematic Window* to close the window.

Select **Session - Quit** on the *Analog Design Environment* form to quit the simulator.

The message "*Do you want to save the current state ?*" will be displayed.

This provides the option to save your simulator settings if required.

Select **No** to complete the quit operation without saving.

Select **File - Exit** on the CIW to exit Cadence.

The message "*OK to exit icfb?*" will be displayed.

Select **Yes** to complete the exit operation.

Click on the **-** icon at the top left of the UNIX Module terminal window.

Select **Close** from the pull down menu.

Select **File - Quit** in the *Transport Window* to close the window.

You can leave the UNIX terminal window open for your next session.

Now click on the **System -> Logout menu** on the to logout.

Confirm the logout when requested.