

**Walkthrough 1  
Standard Cell Design  
Entry and Simulation of Standard  
Library Components**

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## 1 Introduction

This document is intended to replace the digital Design Kit to Verilog exercise in the current 4407. The changes in the licensing structure. Whilst sub optimal in terms of course development the intention is to replicate the functions covered in the original walkthroughs

Compared to the original walkthrough the change are:

**Table 1:**

Change	Original	Update
Design Kit	Mietec 2um	AMS 0.35
Simulator	Verilog	NCVerilog
Environment	Unix Direct	UNIX/Linux Transport
Design Environment	4.1	4.5/4.6

## 2 Conventions used in this document

The following are conventions that will be used in this document.

- Where user input is required it will be delineated with "<>".
- Where a special function key such as escape, control or return/enter is indicated in a command it will also be enclosed in "<>" brackets. For example "<RETURN>".

- Please be aware of spaces in words and commands. Like Windows and common English UNIX and Linux require spaces between commands.
- Unix and Linux commands are lower case unless stated. Unix and Linux are case sensitive.
- Operations involving the mouse will use the left hand mouse button unless otherwise stated.
- Options selected from sub menus will be indicated in the following manner

Main Menu Item -> Sub menu Item -> Sub Menu Item

- e.g. File -> New -> Library

### 2.1 Entering Parameters for commands

Unlike windows most UNIX/Linux parameters are delineated by a "<SPACE>". For example

- `grep -i fred *.v`

## 3 Accessing and Configuring the Design Environment

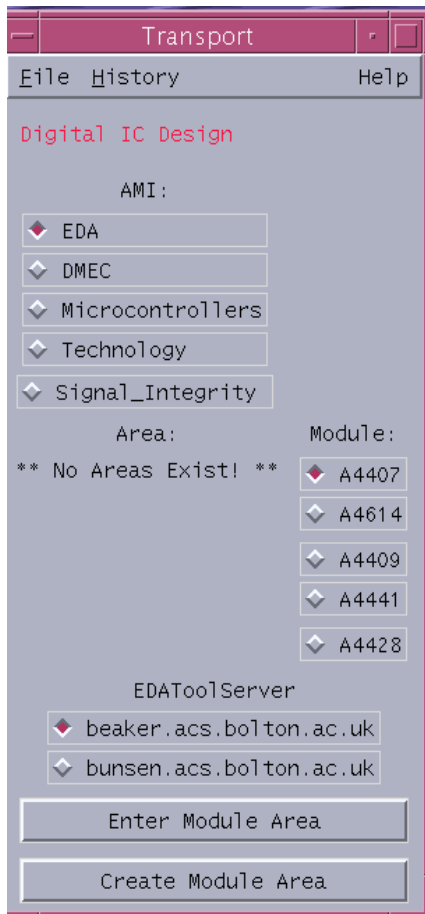
### Creating a Design Environment

Students using the AMI design system are provided with a Transport menu that facilitates easy access to appropriate design directories and associated applications software.

Accessing and Configuring the design environment is achieved using the "transport" tool. Students should start a UNIX terminal window and invoke the transport tool by typing the command:

- `transport & <RETURN>`

The *Transport* form should appear as shown below.



**Fig: Transport Menu with no module areas created for A4407**

The menu enables a module design area to be created and then entered by specifying the module being studied. Modules are classified by type and function.

### 3.1 Using the Transport Form

Click on the **EDA** button to display a list of modules within that classification.

- Select the module **A4407**

If you are using the transport tool for the first time for this module there will be no design areas present and the “Area” field will be blank. In this case you will need to create the default structure by using the “Create Module Area” button.

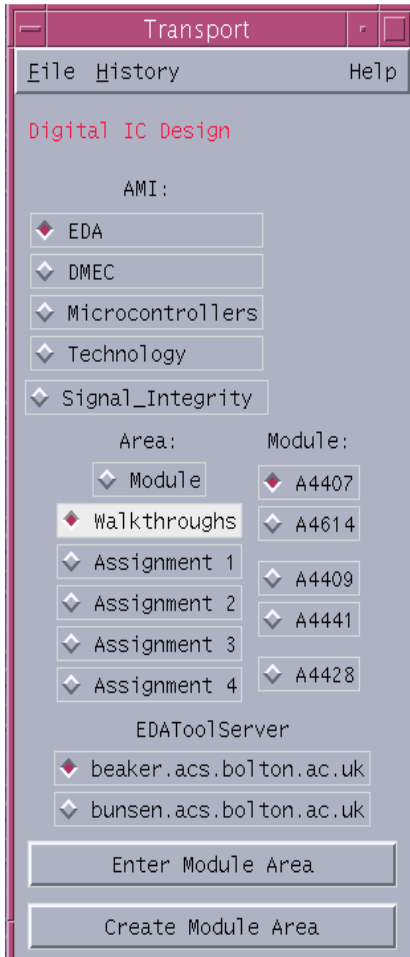
- Click on the **Create Module Area** button to the design areas.

This may take a few seconds. Once this has run successfully the “Area” field will be populated. As shown in the figure “Transport Menu with module areas specified”.

Now select the Walkthroughs area. Only the *Walkthroughs* area will be used for this exercise.

- Click on the **Walkthroughs** button

The *Transport* menu should now be as shown below.



**Fig: Transport Menu with module areas specified**

Now click on the **Enter Module Area** button to open up a configured UNIX terminal window. All subsequent commands will be typed in this window. This window will be in the correct location, in this case the "Walkthrough" area. For the 4407 module this will be physically located at "~/AMI/A4407/Walkthroughs". This area is also configured to allow you to run all the relevant tools and

## 4 Starting Cadence and the AMS 0.35um Design Kit

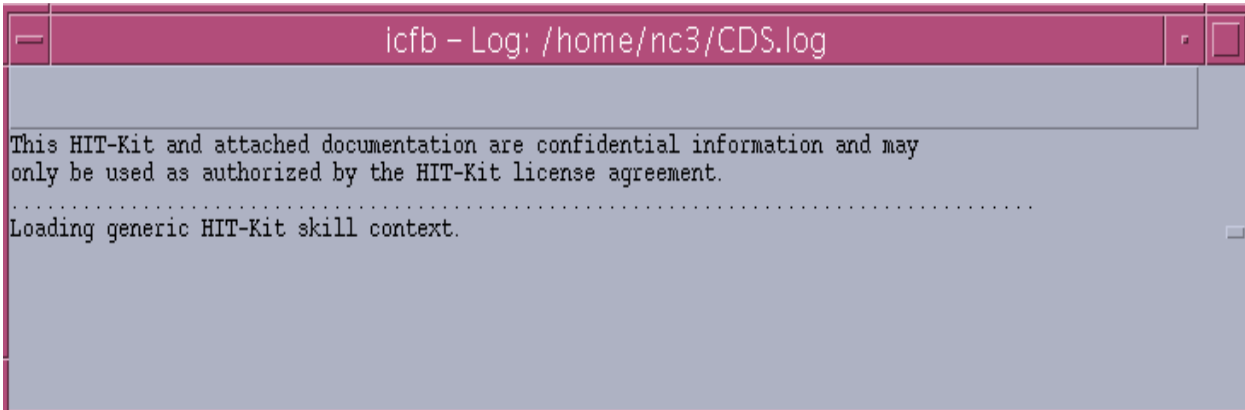
In the configured 4407 terminal window you can start the design kit using the UNIX command:

- **amiselect fb <RETURN>**

After a short delay the CADENCE Command Interpreter Window (CIW) as shown below will appear at the bottom of the screen. The window provides a tool bar for the top level menu commands and a

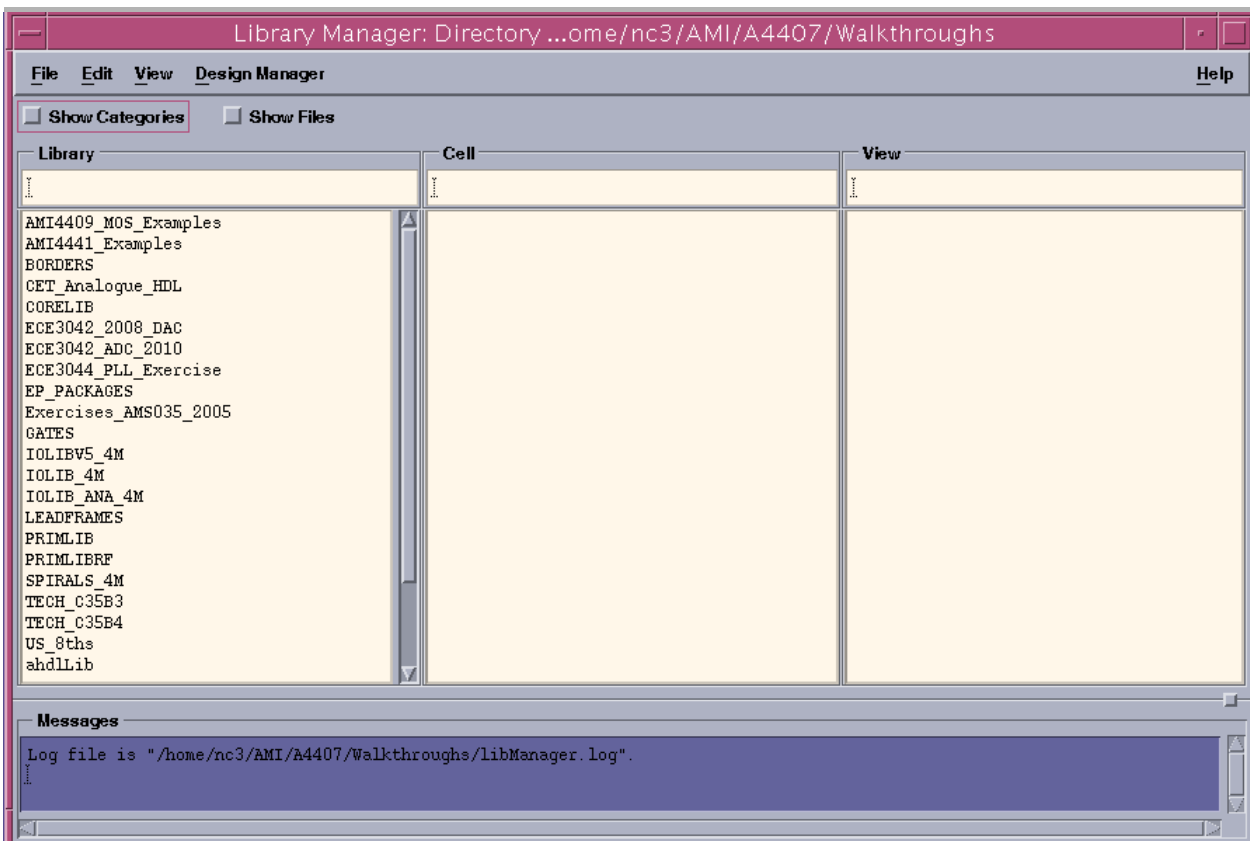
## Entry and Simulation of Standard Library Components

display window for status information.



**Fig: The CADENCE Command Interpreter Window (CIW)**

The Cadence *Library Manager* as shown below will also be displayed.



**Fig: Library Manager**

The *Library Manager* enables design libraries, cells and cell views to be created, opened, copied, deleted and renamed. Amongst other functions.

## Entry and Simulation of Standard Library Components

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### 4.0.1 Library Context Sensitive Menus

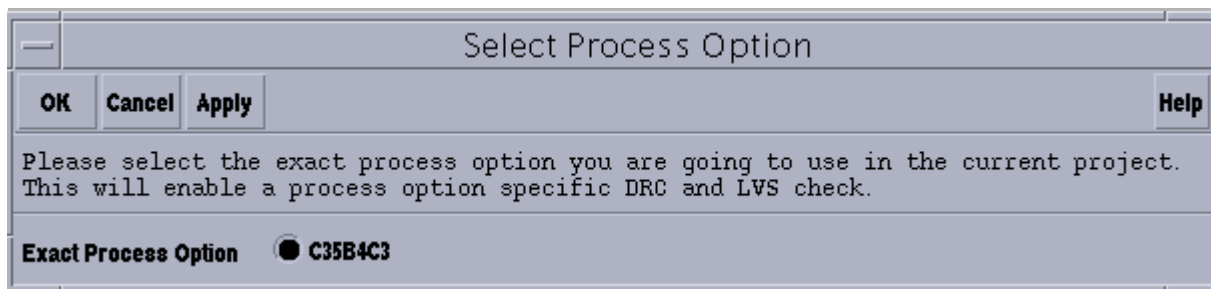
Context sensitive menus are invoked by using the right mouse button. Once you have selected the relevant level i.e. library, cell, cellview.

### 4.0.2 Warning: Make sure you set the process selection form!

If this is the first time that Cadence has been invoked in this module area you may also see a *Select Process Option* form requesting a fabrication process to be defined. Select the default process option (C35B4C3) by clicking on the “OK” button.

- Select the C35C4C3 option and OK the form

The first time you start a AMS design library you will be prompted to select the required design flow. This is done using a blocking mode form. Which means that no further actions can be taken in the Cadence environment. **This form has a habit of being hidden behind the CIW and/or Library form.** The first time you invoke the amiselect command to create the design area make sure that you locate and select the relevant option on this form. If you cannot see it then iconise the other forms and windows.



**Fig: Select Process Option form**

“OK” the form and you can continue working.

## 4.1 Using the Design libraries

CADENCE defines a design database as a series of libraries, some containing components supplied by the device manufacturer (e.g. resistors, capacitors, transistors etc.) and some generated by the designer. These components are referred to as cells.

We need to create our own library and cells to implement our design. The following provide an outline of the steps required. Our design will define a cell named *test1* in a library called *examples*. From the *Library Manager* select the following menu option:

- **File - New - Library** to display the *New Library* form.

Click in the *Name* box, enter the library name **examples**, or anything else that takes your fancy.

The completed form should be as shown below with your own path and name in the lower box.

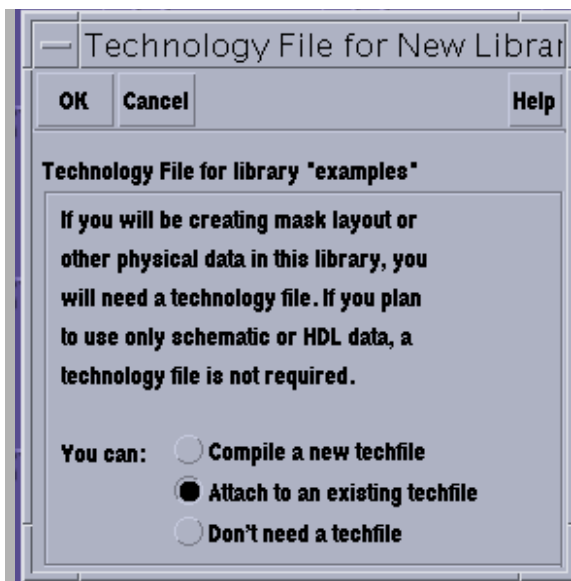
The image shows a 'New Library' dialog box with the following fields and options:

- Library Name:** examples
- Directory:** ..
- Design Manager:**
  - Use NONE
  - Use No DM
- Buttons:** OK, Apply, Cancel, Help

**Fig: The Completed New Library Form**

Accept the form by clicking on **OK**.

- A *Technology File For New Library* form will now be displayed. Click on the **Attach an existing techfile** button as shown below. The Completed Technology File Form should resemble the one below



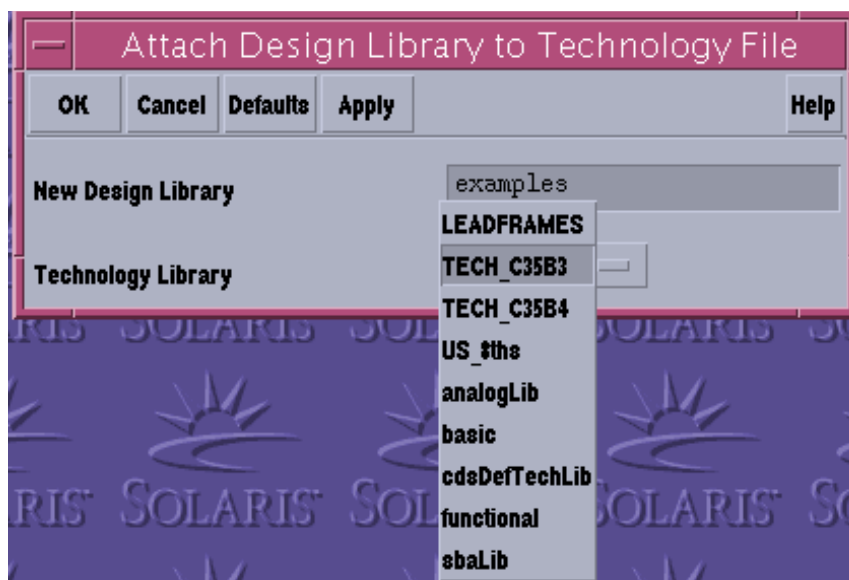
**Fig: Selecting to use an existing technology file**

Click on **OK** to open the form to select the technology library.

When the "Attach Design Library To Technology" form appears use the "Technology Library" cyclic field to select the "TECH35CB3" technology library.

Select the TECH\_C35B3 technology Library.

Click **OK** to select the technology library.



**Fig: Technology Library Attachment Form**

A message will appear in the CIW confirming successful creation of the library

The library name *examples* will also have been added to the library list in the first column of the *Library Manager*.

## 5 SCHEMATIC ENTRY

### 5.1 Introduction

This section details the operating instructions for invoking CADENCE and running *Composer* to enter the stepper motor driver schematic.

Instructions are provided for entering logic components, input/output pins and wires and for checking and saving the design.

### 5.2 Creating a schematic Cellview called test1

Click on the **examples** library in the *Library Manager* and verify that it highlights.

Select **File -> New -> Cellview** from the *Library Manager* to display the *Create New File* form.

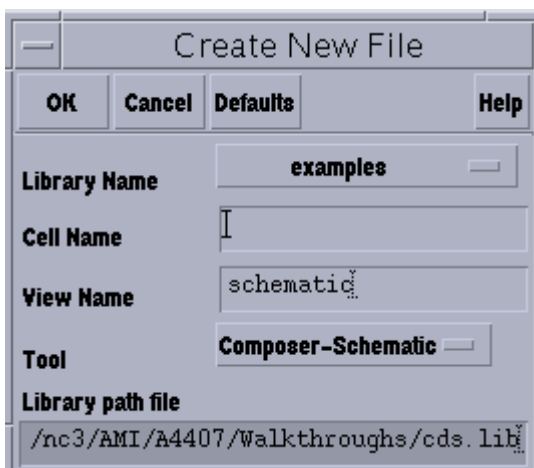
Click in the *Library Name* box to display the list of available libraries.

Select **examples** from the list.

Click in the *Cell Name* box and enter **test1** as the cell name.

Verify that the *View Name* box has been set to **schematic**.

Verify that the *Tool* box has been set to **Composer -Schematic**.



**Fig: The Create New File form**

Add in the entries for the cell name and accept the form by clicking on **OK**.

A message will appear in the CIW confirming successful creation of the cellview and an empty

## Entry and Simulation of Standard Library Components

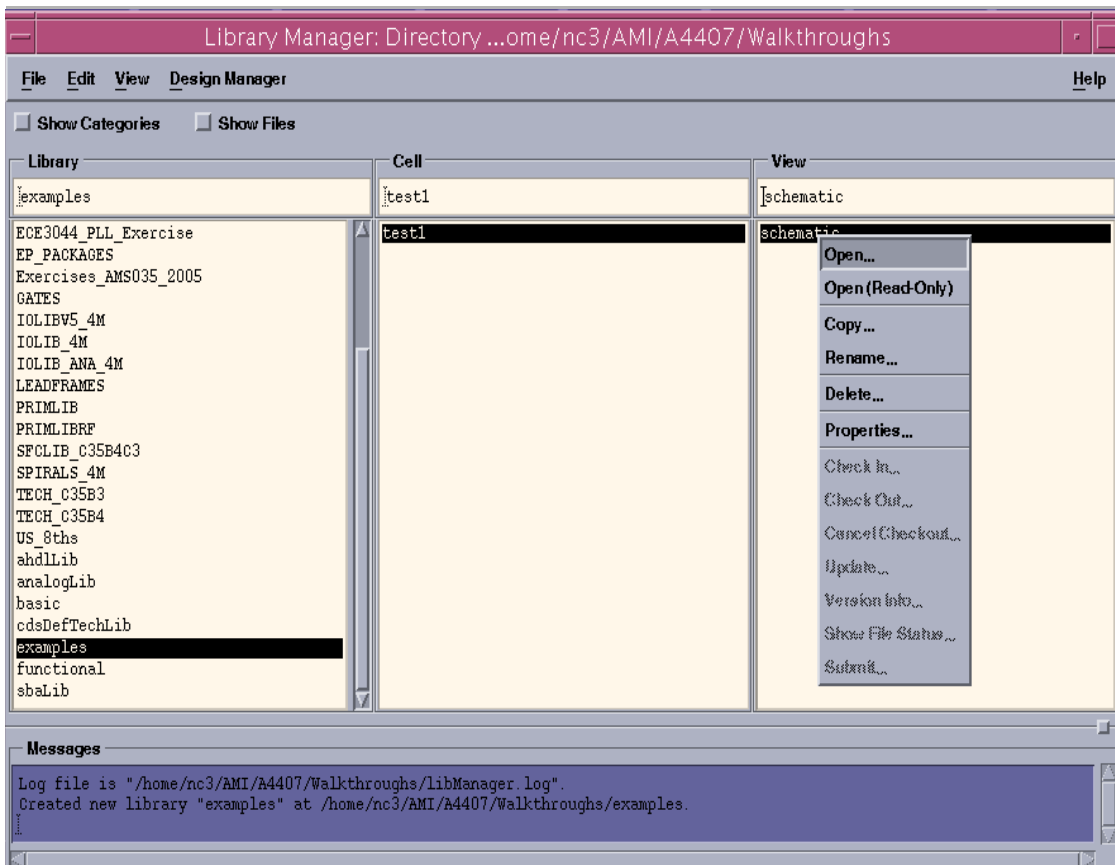
schematic window will now open.

### 5.2.1 Supplementary Information

Note: In subsequent sessions should you wish to display or edit the schematic that you are about to create you can select it either from the CIW or via the Library manager. The recommendation would be to use the Library manager

From the *Library Manager* select the required *Library Name* (**examples**), *Cell Name* (**test1**) and *Viewname* (**schematic**) as shown below

Select **File - Open** from the *Library Manager* to open the schematic, or right click on the schematic view to bring up the context sensitive options.



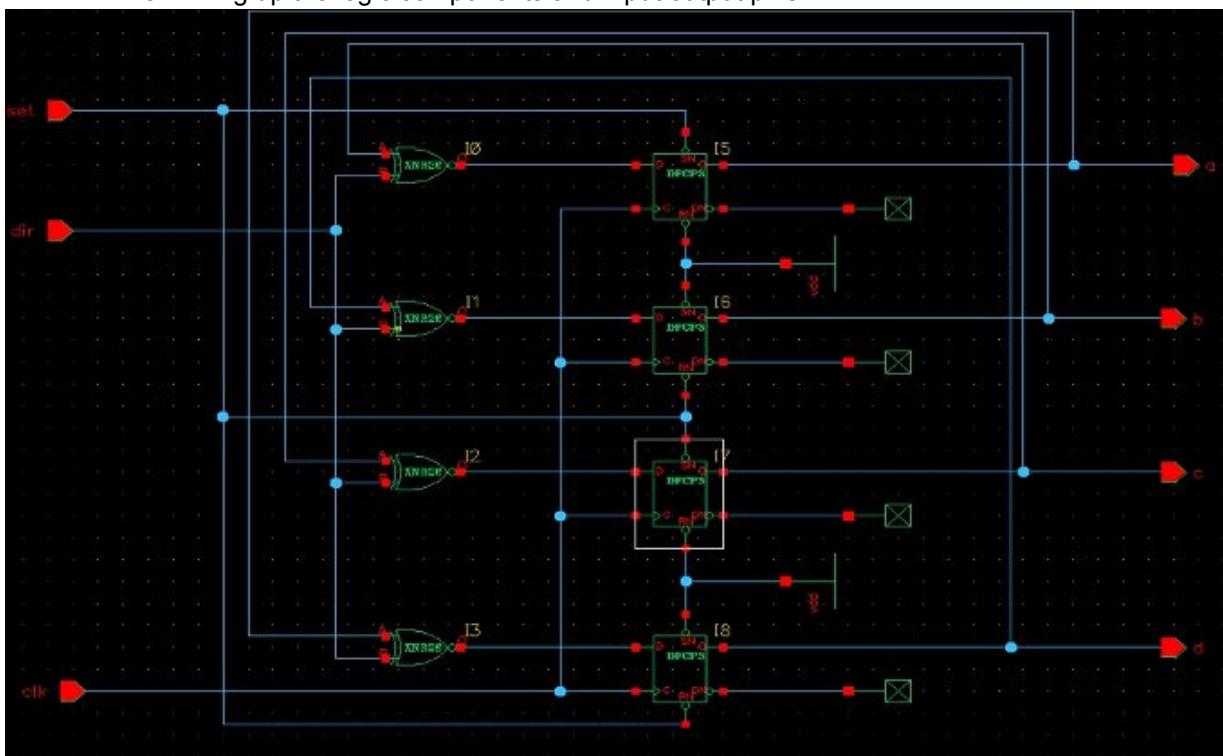
**Fig: Selecting the test1 schematic from the library browser**

## 6 Entering the Schematic

The schematic window displays the main options along the top and a subset of these options in icon form down the left hand side.

The circuit schematic shown below will be assembled in three stages:-

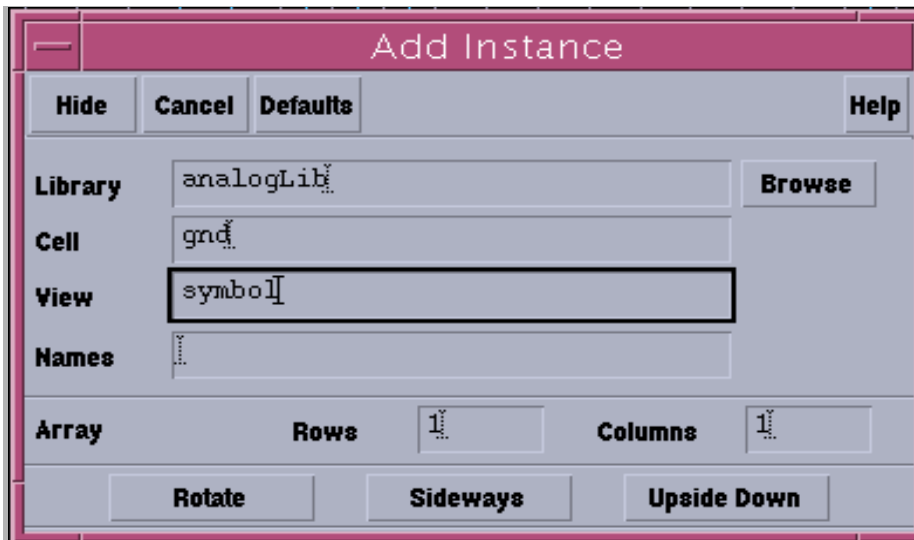
1. Enter the logic components
2. Enter the input and output pins
3. Wiring up the logic components and input/output pins



**Fig: Final Schematic**

### 6.1 Entering the Logic Components

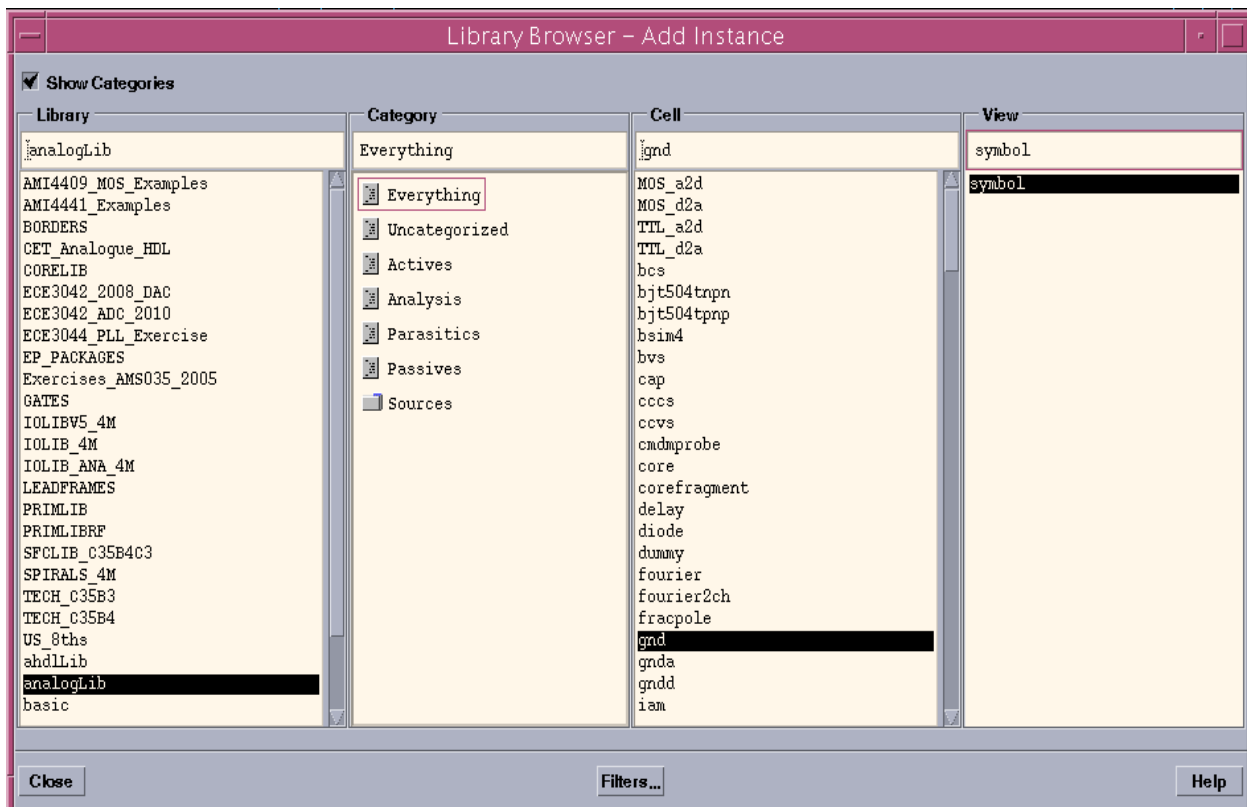
Select Add - Instance (or use the i key on the keyboard) to display the *Add Instance form* as shown below.



**Fig: Add Instance Form**

Select the *browse* option to open the “Library Browser - Add Instance” form. This form should resemble the one shown below.

- Hint: Be careful not to confuse this with the normal Library browser form the functions are different.



Note that the “Show Categories” option is on. Indicated by the tick in the top left hand corner.

### 6.2 Schematic Components

The following components were used to construct the schematic. Please note that schematic pins are not library components and may be added using the Add->Pin or associated icon. Their use will be described later.

**Table 2: Schematic Library Components**

Library	Name	View to use
analogLib	vdd	symbol
Basic	noConn	symbol
CORELIB	XNR20	symbol
CORELIB	DFCP3	symbol

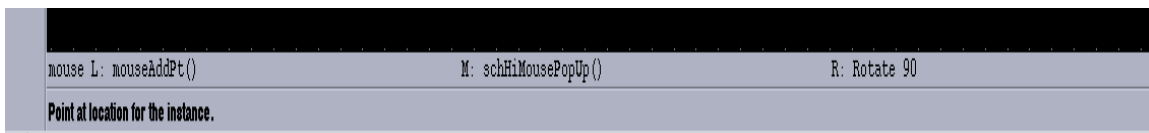
Use the mouse to navigate “Library Browser - Add Instance” form and select the cell and cell view required. It is suggested you select the DFCP3 from the CORELIB library first.

The DFCP3 component will now be attached to the cursor in the schematic window. At this point you may wish to move the *Library Browser* out of the way to facilitate the placement of the component. Simply press and hold down the left hand mouse button in the window title bar and drag to the required location.

Now position the component where required in the schematic window and click the left hand mouse button to place and instance in the required location.

Press the <ESCAPE> key to terminate the Add Instance option and release the component from the cursor. In fact the majority of operations can be terminated using the <ESCAPE> key.

Hint: If you are unsure of the selected function look at the base of the schematic window. The function of the left, middle and right mouse buttons is shown.



**Fig: Example of Mouse Functions at Base of Schematic Window**

### 6.2.1 Supplementary Information

#### 6.2.1.1 F3 accessing the Options form for the selected command

Many commands have additional options place instance, copy and move amongst them. These additional options form can be called up using the F3 button. This also allows you to hide the additional options form as well.

#### 6.2.1.2 Zoom In/Out/Fit

There are a number of zoom options available by bindkeys of via the Window->Zoom option

**Table 3: Useful Zoom options**

Menu	Bindkey	Function
Window->Fit	f	Fit
Window -> Zoom in by 2	]	Zoom in X2
Window -> Zoom out by 2	[	Zoom out X2
Windows Redraw	F6	Refresh Window
Scroll View Left/Right	CursorKey Left / Right	
Scroll View Up/Down	Cursor key Up/Down	

### 6.3 Creating the schematic

It may also be necessary to zoom out/in the display before placing further components. Select Window - Zoom Out By 2 from the schematic window menu repeatedly until the required display size is achieved.

You may wish to use the keys fit, “[“and “]” to zoom in and out to make the work easier.

Place another three instances of the DFFSLRL component.

This can be done in any of the following ways:-

Repeat the Add Instance procedure as detailed above for each instance

Select Add Instance mode but when a component has been selected and placed simply re-position the cursor to the required position for another instance and place by clicking the mouse button. When all instances have been placed terminate the option using the <ESCAPE> key.

Copy an existing instance by selecting Edit - Copy (or the c key) and clicking on the

component to be copied. A copy of the component attached to the cursor will highlight. Position the component in the required location for the copy and click again to fix in position. Terminate the option using the <ESCAPE> key.

### 6.3.1 Practising a stretch, move, delete and undo operation

As the component entry proceeds it may be necessary to move and delete components if mistakes are made. Before continuing we will practice moving and deleting one of the DFFSLRL components.

#### 6.3.1.1 Select

Select the component by clicking on it. It should now be surrounded by a white border. This is the bounding box. In schematics it is usual for all pins to lie along the border box. When you move the mouse over the instance the border will be initially yellow dotted. If you click this will turn white. You can select multiple items or areas by holding the left hand mouse button down and drawing a rectangle.

#### 6.3.1.2 Move and Stretch

There are two types of move Edit->Stretch, bindkey lowercase m, and Edit -> Move, bindkey capital M. The difference is that a Stretch will retain any wire connectivity whilst a Move will not retain an wire connectivity.

Move the component by selecting Edit - Move (or M on the keyboard) and clicking on the component to be moved. The component attached to the cursor will highlight. Position the component in the required new location and click again to fix in position. Terminate the option using the <ESCAPE> key

#### 6.3.1.3 Delete

Delete the component by selecting Edit - Delete (or the Delete key) and clicking on the component to be deleted. The component will now be removed. Terminate the option using the <ESCAPE> key

#### 6.3.1.4 Undo

Restore the component deleted by selecting Edit - Undo (or the u key). The undo command effectively cancels the last operation.

Now place the remaining components. Which are the XNR20, vdd and noConn. Table 2 defines the location of these components.

The schematic should resemble that shown below

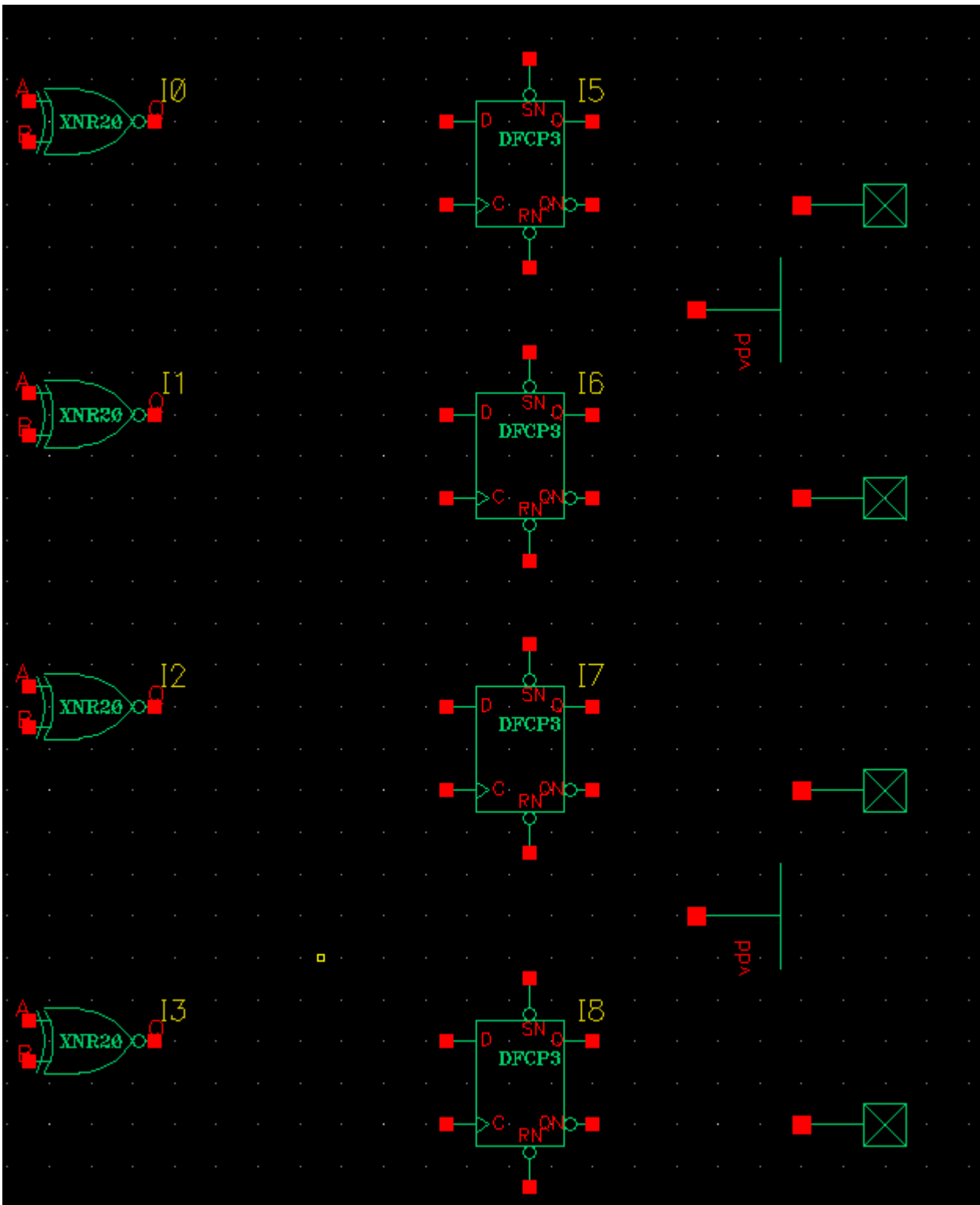


Fig: Figure 8 The Schematic

### 6.4 Entering the Input/Output Pins

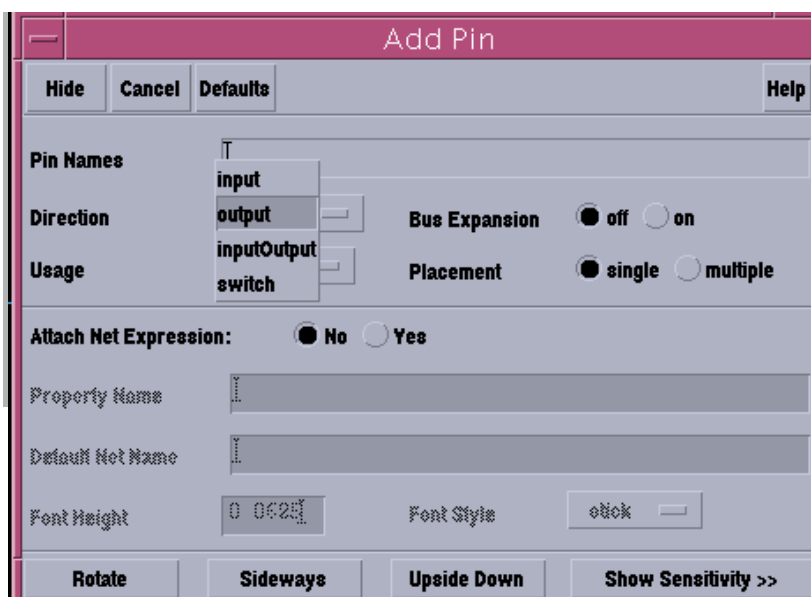
The input and output pins are defined as follows:-

Signal Name	Type	Function
reset	input	driver reset
dir	input	forwards/backwards select
clk	input	driver clock
a	output	motor winding a
b	output	motor winding b
c	output	motor winding c
d	output	motor winding d

Zoom into the area surrounding the XNR20 gate in the top left hand side of the schematic by selecting Window - Zoom In (or the z key). Position the cursor at the top left of the zoom area and press and hold the left hand mouse button. Drag the cursor to the bottom right of the zoom area and release the mouse button. The selected area will now be enlarged.

At any time you can revert to the full window view by selecting Window -> Fit (or the f bindkey).

Now select Add -> Pin (or the p bindkey) to display the Add Pin form as shown below.



**Fig: Figure 9 The Add Pin Form**

## Entry and Simulation of Standard Library Components

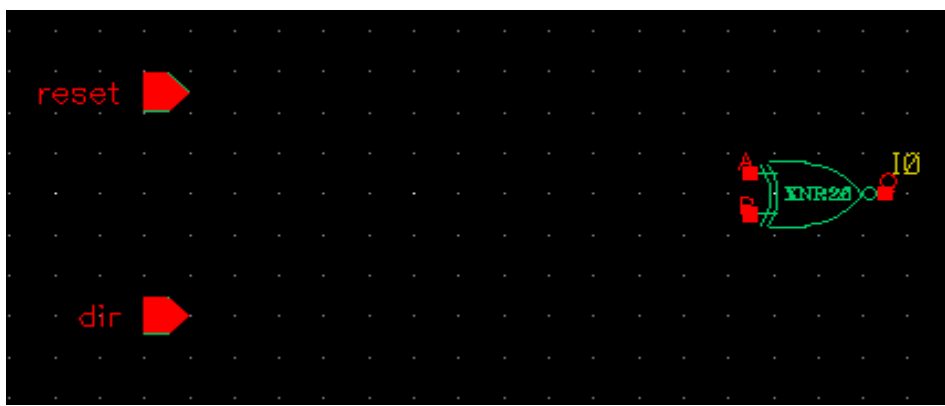
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### 6.4.1 Entering the inputs pins

Make sure the direction field of the form is set to input

Select the form and add either one or all of the input pin names into the box, separated by spaces. If using multiple pins then one mouse click will place one pin.

Enter the pin name reset into the Pin Names box and terminate the input by pressing the RETURN key. An input pin symbol will now be attached to the cursor. Locate the pin as detailed in the circuit diagram at the beginning of the walkthrough and click to fix in position. Check that the pin name is displayed adjacent to the pin as shown below.



**Fig: Pin Placement Example**

Repeat the procedure for the dir and clk input pins referring to the circuit diagram (dir connects to the top Exclusive NOR gate and clk to the clock input of each flip-flop)

Entering the output pins

Note: Input/Output pins can be deleted and moved using the same procedure as for components.

Follow the same procedure for the output pins referring to the circuit diagram (pin a connects to the top flip-flop output and pins b, c and d follow down in sequence).

Make sure the direction field is set to output before placing the pins.

## 6.5

### Repositioning and tidying up the schematic

At this stage you may want to reposition some or all of the components. Given the potential run of the wiring interconnects required. This is most easily accomplished by using the group move facility.

#### 6.5.1 Select Edit - Move (or the M key).

Position the cursor at the top left hand corner of the group of components to be moved. Press and

## Entry and Simulation of Standard Library Components

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hold down the left hand mouse button and drag the cursor to the bottom right hand corner of the group. A yellow box will appear encompassing the components. Release the mouse button and all the components will highlight in white indicating that all have been selected. Click anywhere in the group to define a reference point and move the group to the new position. Click again to fix in the required location.

### 6.5.2 Supplementary Information

This facility can also be used with the Edit - Delete operation but caution is advised!

## 6.6 Wiring the Components

There are two methods of connecting components depending on their relative positions.

### 6.6.1 Automatic Connection

The connection between the input pin reset and the inverter is an example.

Select Add - Wire (narrow) or the w key.

Click on the input pin named reset to define the wire source. The wire will now be attached to the cursor. Click on the input terminal of the inverter to establish the wire destination and the wire will now be connected.

### 6.6.2 Manual Connection

This allows you decide on the location of the “corners” for the wires.

Click on the output terminal of the inverter and guide the wire by clicking on each required horizontal/vertical turning point until the wire destination is reached.

Repeat for the remainder of the wires as detailed in the circuit diagram

Cancel the Add Wire operation when you have completed all the connections by pressing the Esc key.

### 6.6.3 Supplementary Information

Wires can be removed using the Delete option.

Wires can be moved using the Stretch option.

Select Edit - Stretch (or the m key)

## Entry and Simulation of Standard Library Components

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Click on a segment of the wire to be moved, move to the required position and click again to fix the location.

### 6.7 Checking and Saving the Design

The design must be checked for schematic errors before saving in the database.

Select Design - Check and Save (or the X key).

Inspect the CIW for any errors and warnings that may have been reported. Expect four warnings relating to the unconnected inverse outputs of the flip-flops. These will flash on the schematic but can safely be ignored.

Errors however must be corrected. As for warnings the offending components or wires will be highlighted on the schematic for reference. Correct the errors and repeat the Check and Save operation until the schematic is error free.

Hint: The most common error is usually to not fully connect to a pin.

Hint: You can use the Check -> Find Marker form to zoom between the errors on your schematic. The CIW will list the errors, and it a yellow blinking box will surround the error on the schematic. However on larger schematics this can be a tad small and in this case the Check -> Find Marker tool is used. Select the "Zoom to Markers" option and control the zoom size to make life easier.

## 7 GATE LEVEL SIMULATION

### 7.1 Introduction

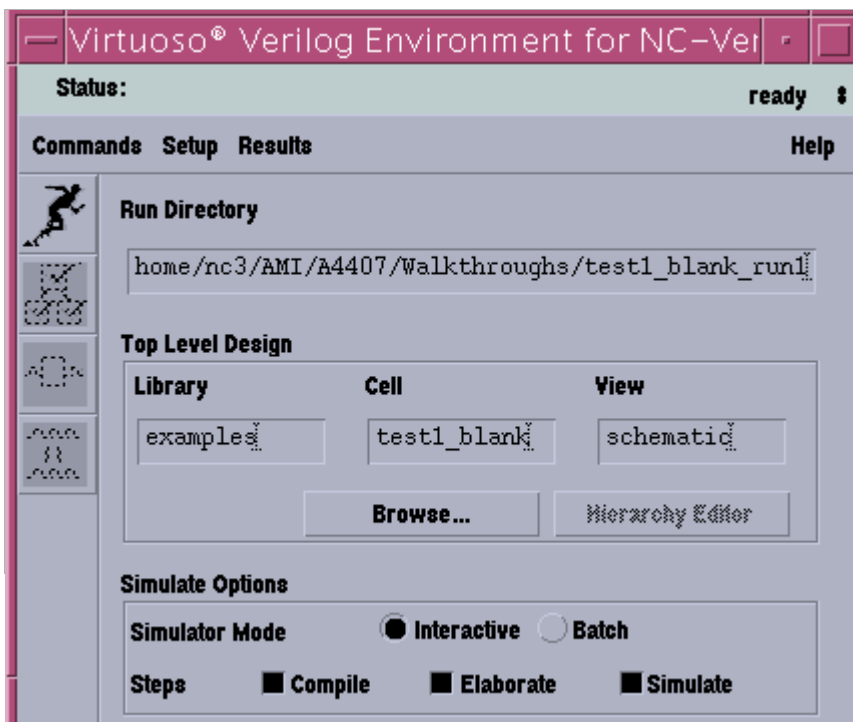
This section details instructions to simulate the driver circuit.

Instructions are provided to create a testfixture file for the simulation test vectors, run the Verilog simulator and display graphically the output results.

### Starting the Verilog Simulator

Select Tools - Simulation -> NC-Verilog from the schematic window.

The *Virtuoso Verilog Environment for NC-Verilog* form will be displayed.



**Fig: Starting the Verilog Simulator**

From this we can start and control the simulation. You will notice that the form is already filled in with the relevant details. Should we wish to change to another schematic we can use the Browse option to do so.

A considerable amount of configuration is provided by the design kit environment to ensure that such simulations are relatively straight forward. For example VDD will be recognised as a logic 1, whilst VDD would be recognised as a logic 0. The hierarchical netlist views are also configured to provide the requisite digital views and to access the relevant netlist files for the Verilog models.

### 7.2 Initialising the Environment

Select the Commands -> Initialize from the Virtuoso Verilog Environment form, or use the “Running man” icon. This will initialise the environment. Check the CIW window to ensure this was successful.

### 7.3 Generating the Netlist

The next step is to generate the netlist. This will also produce the testfixture template files that we will require to generate the test pattern for the device.

Select the command Commands->Generate Netlist, or the relevant icon. Again check the CIW window for successful completion.

Hint: The most usual issue is that the schematic has not been checked and saved. Even something

## Entry and Simulation of Standard Library Components

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which did not change the schematic can set the “unchecked” flag in the tools. So always do a check and save first.

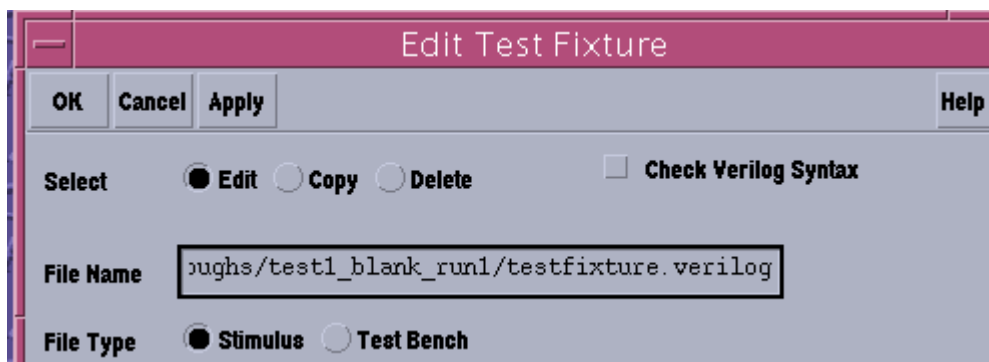
### 7.4 Creating a Stimulus Testfixture Template

A stimulus testfixture template can be generated from the schematic.

This form will be regenerated anew each time the “Generate Netlist” option is used so we need to avoid having to re-enter our work. We will discuss this later in this exercise.

Select the Commands -> Edit Test Fixture option.

This will display the “Edit Test Fixture” form.



**Fig: Edit Test Fixture Form**

Notice the button settings of “Edit” and “Stimulus”.

Select OK to open the Stimulus file generated by the netlist operation for edit. The file should resemble the listing below:

- // Verilog stimulus file.
- // Please do not create a module in this file.
- // Default verilog stimulus.
- initial
- begin
- clk = 1'b0;
- dir = 1'b0;
- reset = 1'b0;
- end

### 7.5 Editing the Stimulus file

Now open the "testfixture.verilog" file for edit. We need to add in the required stimulus to drive

the inputs of the test circuit.

Add the following stimulus data so that the file contents are as shown below. You can cut and paste if you wish.

```
// Verilog stimulus file.
// Please do not create a module in this file.

// Default verilog stimulus.

initial
begin
    clk = 1'b0;
    dir = 1'b0;
    reset = 1'b1;
end

always #50 clk = ~clk;

initial
begin

    #100    reset=1'b0;
    #100    reset=1'b1;
    #500    dir=1'b1;
    #500    $finish;
end
```

### 7.5.1 Explanation of the stimulus declarations

The timescale declaration in the testfixture.new file is 1ns/1ps. Hence any integer value entered is in ns. With a resolution of ps. For example 1.001 would be possible. 1.0001 would not in terms of accuracy. Verilog used to have a 32 bit time counter limit in the early days but this has long since passed into history.

- **always #50 clock=~clock;** - Defines a clock with a 50 ns toggle rate [i.e. a clock period of 100 ns]
- **dir=1'b0; reset=1'b1;** - Sets the specified signals to their initial logic values at time 0.
- 
- **#100 reset =1'b0;** - Sets the reset signal to logic 1 at 100ns after the start of simulation  
**#100 reset =1'b1;** - then logic 0 at100ns later.
- **#500 dir=1'b1;** - Run the simulation for 500ns then set dir to logic 1
- **#500 \$finish;** - Stops the simulation 500 ns later.

In this mode all times are cumulative rather than absolute.

The **initial** declarations are used to set time to zero before each new set of data.

Select File - Save from the editor window to save the file contents.

(The editor window can be closed by selecting File - Close but it is recommended that it is left open for the moment in case modifications are required to the file).

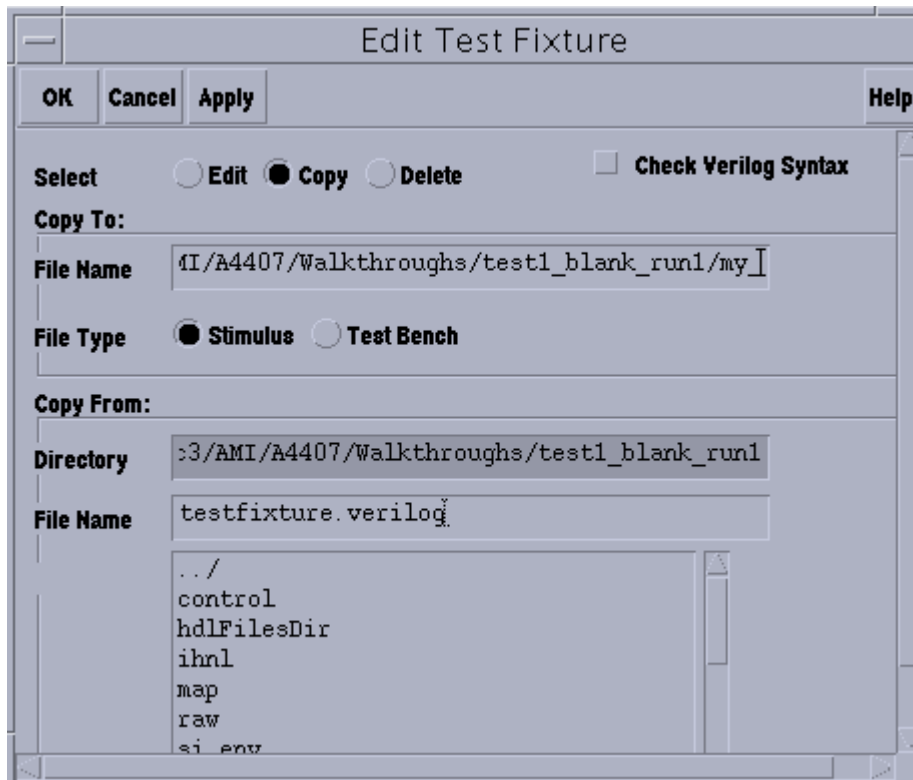
Hint: When correcting errors in the stimulus files it is not necessary to regenerate the netlist.

### 7.6 **Avoiding overwriting the stimulus file by copying the testfixture.verilog file and using it in the simulation.**

If you renetlist then the stimulus file will be overwritten and if you have not saved it or retained it in an open editor then you will have issues. Those of you who are adept should actually be able to do the whole thing using the text editor invoked for the stimulus file and selecting the relevant files by name.

The following is the more complex procedure that avoids this situation, that utilises the "Edit Test Fixture" form.

- Ensure the setting on the EDit Test Fixture form is "Stimulus"
- Open testfixture.verilog for edit
- Save testfixture.verilog to a new file e.g. my\_testfixture.verilog
- Edit the new file as required.
- Change the setting on the Edit Test Fixture form from "Stimulus" to "Test Bench"
- Edit the testfixture.verilog
- Change the line:
  - `include "testfixture.verilog"`
  - To point to your verilog of the test fixture file e.g.
  - `include "my_testfixture.verilog"`



**Fig: Figure Edit Test Fixture form in Copy mode**

The name you chose must be unique and not clash with any existing files in the directory.

Supplementary Information: As the files are stored in the simulation directory, which is generated from the cell name and by default is in the same directory as tools were invoked. Removing/overwriting the simulation directory can cause you to lose the files. It is for this reason that when using this technique the files are never stored in the simulation directory. An include file as part of the verilog options is used to provide access to such files. Usually stored in a revision controlled area. Even testfixture.new is untrustworthy when you create a new area. There are different approaches and levels of usage dependent on experience and environment.

### 7.7 Initialising and Running the Verilog Simulator

Select the Commands -> Simulate option, or the appropriate icon. This will start the simulation and invoke the simvision tools environment. It may take a few seconds for the windows to appear.

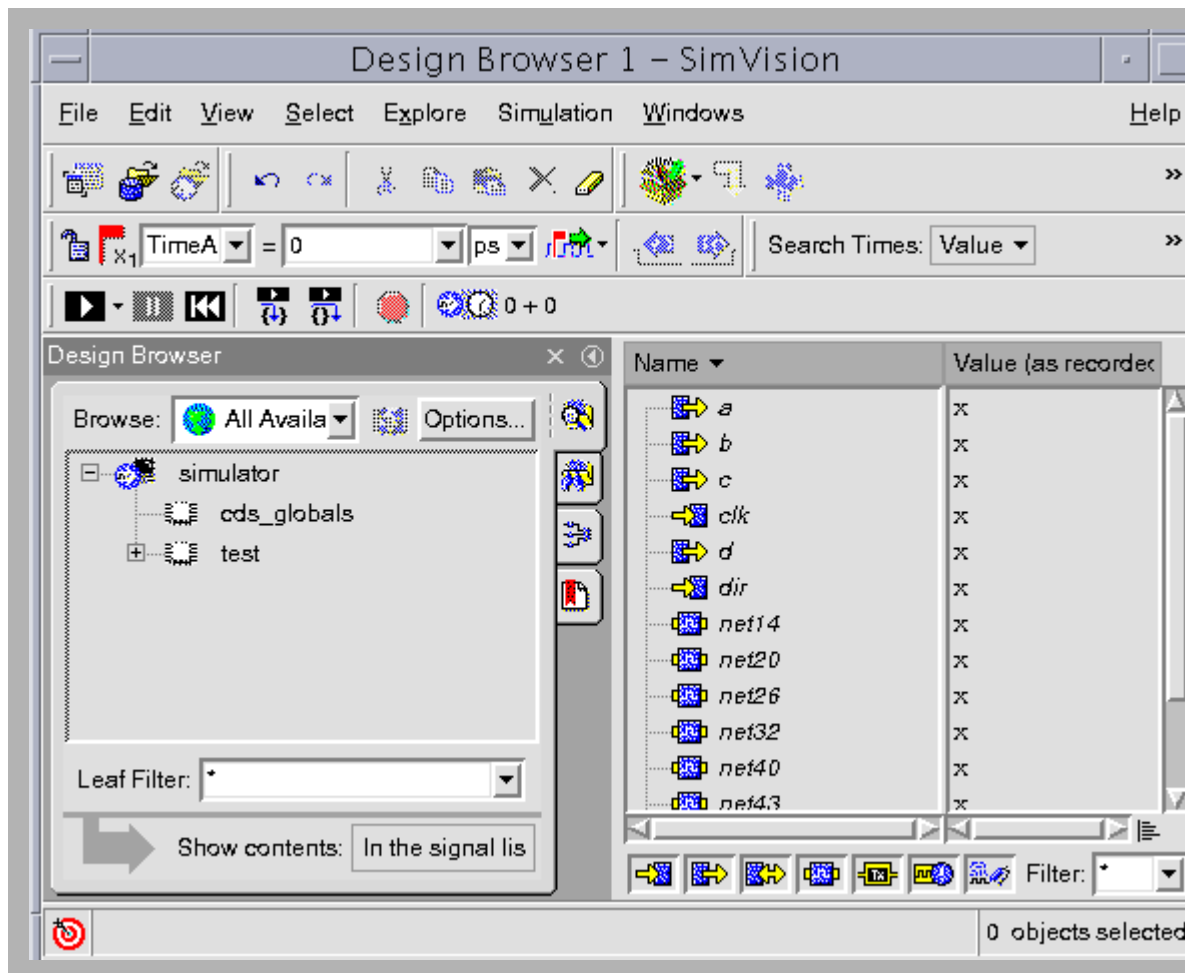
### 8 Simvision

This is the simvision environment. Detailed information on the various consoles and windows are provided as appendices to this document. As the intention is to, at least for this cycle of the module to minimise disruption.

### 9 Displaying the Simulation Results

#### 9.1 Selecting the Design Hierarchy

Select the Simvision Design Browser window and in the left hand pane click on the + icon next to the test entry. This will expand out the top level of the design hierarchy. At the same time the right hand pane will fill with the nets and ports on the schematic.



**Fig: Sim Vision Design Browser**

Before the simulation results can be displayed it will be necessary to select the required signals. Move the mouse into the left hand pane and using <CTRL> left mouse click select all the required

signals. <CTRL A> will select all the signals. Once selected a signal will be highlighted in yellow. Now send these signals to the waveform browser by using the right mouse button to bring up the context sensitive menu, whilst the mouse cursor is in the right hand pane. Use the “Send to Waveform Window” option. An alternative is to click on the waveform icon

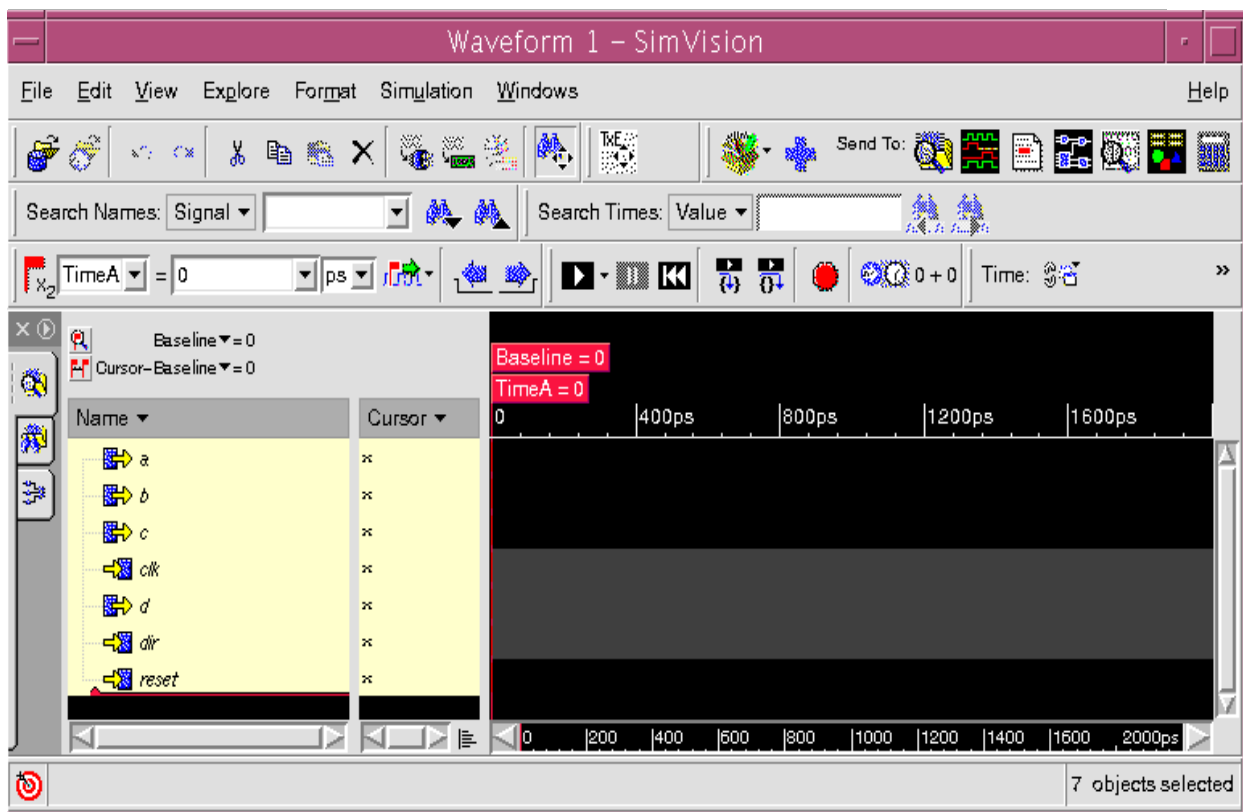


**Fig: Waveform Window Icon**

Signals of interest could include:

- a
- b
- c
- clk
- d
- dir
- reset

## Entry and Simulation of Standard Library Components



**Fig: Waveform window showing selected signals**

### 9.2 . Running the Simulation

We now need to run the simulation. If we select the waveforms after we have run the simulation then there will be nothing to display.

To run the simulation we can use the Simulation -> Run command available on all the SimVision windows.

- Simulation -> Run
- Once we have done this the waveform window should show us the results. We can use the View -> Zoom options or the View icons (on the right hand side) or the bar at the base to move, zoom in/out on the waveforms.

Hint:

We can also reset the simulation to time zero using the Simulation -> Reset to Start command.

We can also using the console window run the simulation for a fixed time by entering “run 20 us”.

There are also a whole plethora of other options as would be expected in a sophisticated IDE environment.

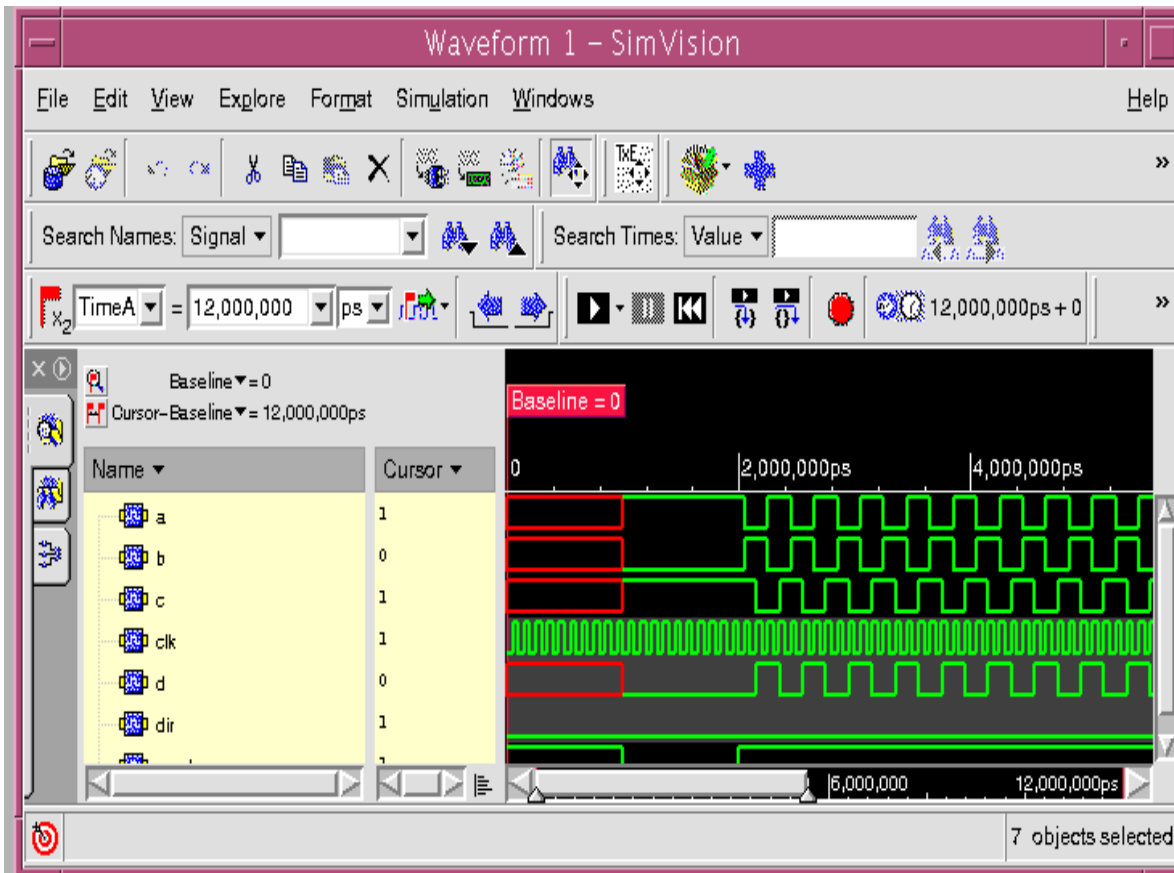
Inspect the waveforms to verify that the circuit is functioning correctly according to the following sequence

**Table 4: Output Sequence for System**

reset	dir	a	b	c	d
0	X	1	0	1	0
1	0	0	1	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	0	1	0
1	0	0	1	1	0
1	0	0	1	0	1
1	0	1	0	0	1

### Determining the Circuit Delays

Whilst propagation delays can be measured from the results of such a simulation. Their relative accuracy is low. As modern technology has gone into what is termed DSM or Deep Sub Micron mode we long ago, approximately 0.25u, passed the point at which track level capacitance delays exceed gate level capacitance delays. For any modern system to provide accurate timing information a PKS, Physically Knowledgeable Synthesis, or post layout SDF, Standard Delay Format, file are required to get accurate timing. The period when delay estimation could be made from the number of gates connected to a net plus an adjustment for net length, and the answer be meaningful are long past I am afraid. Many Verilog simulators had PLI based timing calculators to enhance the load/delay calculations that can be used with Verilog.

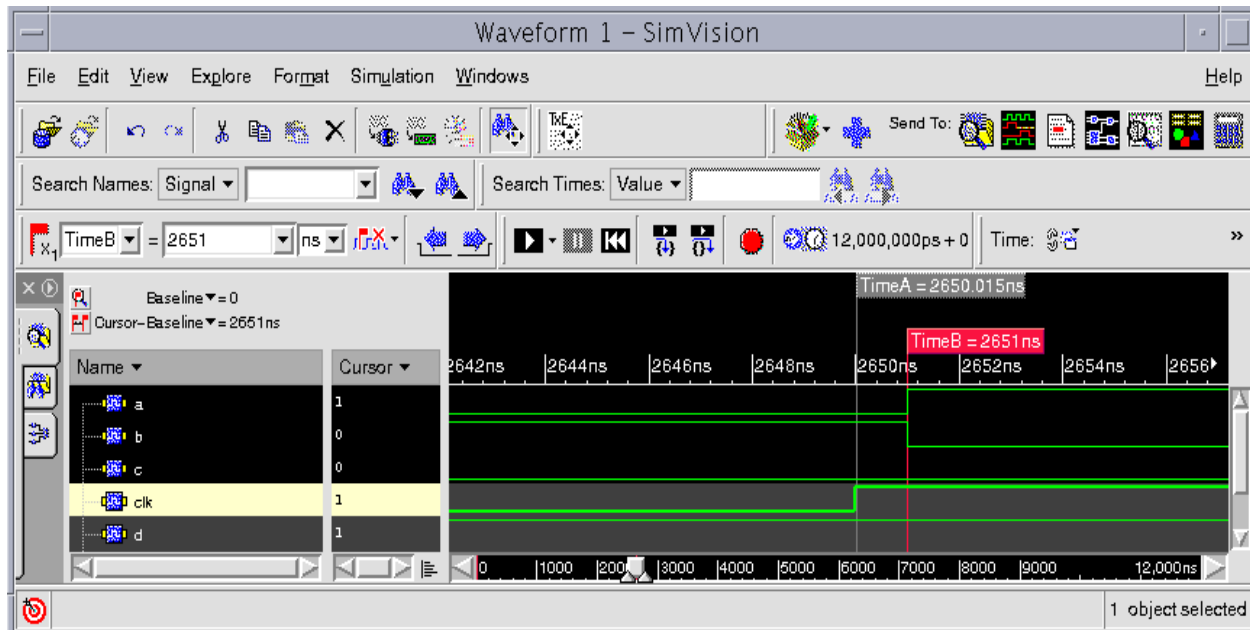


**Fig: Results from Simulation**

9.2.1 Measured Delays

Modern Technologies are also increasingly faster and it can be seen that the estimated clock to output change delay in these circumstances is about 0.985ns.

## Entry and Simulation of Standard Library Components



**Fig: Timing Measurement Example using Simvision1**

Hint: If you look to the top left of the Waveform browser in the figure above you will see a cyclic field showing Time A. Allowing you to manipulate the cursor A. If you use this field you can create as many new cursors as you require to measure items. Further to the right of this field is the time field that sets the overall display resolution. Currently set to ps.

## 10 Leaving CADENCE

Exit from the *Simvision* by selecting File - Exit Simvision on any of the relevant tool panes.

Confirm the action by clicking on Exit when requested

Close down the *Verilog-XL Integration Control* menu by selecting File - Quit

Confirm the action by clicking on Yes when requested

Select Window - Close on the schematic window to close the window.

Select File - Exit on the CIW to exit CADENCE.

The message “OK to exit icfb?” will be displayed. Select Yes to complete the exit operation.