

**Walkthrough 3
Full Custom Using Standard Cells**

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1 Introduction

This document is intended to replace the Entry and Simulation of Full Custom Components in the current 4407. Whilst sub optimal in terms of course development the intention is to replicate the functions covered in the original walkthroughs

Compared to the original walkthrough the change are:

Table 1:

Change	Original	Update
Design Kit	Mietec 2um	AMS 0.35
Simulator	cdsSpice	Spectre
Environment	Unix Direct	UNIX/Linux Transport
IC Design	1999-2000	4.5/4.6
Layout	Virtuoso	Layout XL
Router	LAS	Encounter / Assura

2 Conventions used in this document

The following are conventions that will be used in this document.

- Where user input is required it will be delineated with "<>".
- Where a special function key such as escape, control or return/enter is indicated in a command it will also be enclosed in "<>" brackets. For example "<RETURN>".
- Please be aware of spaces in words and commands. Like Windows and common English UNIX and Linux require spaces between commands.
- Unix and Linux commands are lower case unless stated. Unix and Linux are case sensitive.
- Operations involving the mouse will use the left hand mouse button unless otherwise stated.
- Options selected from sub menus will be indicated in the following manner

Main Menu Item -> Sub menu Item -> Sub Menu Item
- e.g. File -> New -> Library

2.1 Entering Parameters for commands

Unlike windows most UNIX/Linux parameters are delineated by a "<SPACE>". For example

- `grep -i fred *.v`

3 Accessing and Configuring the Design Environment

Creating a Design Environment

Students using the AMI design system are provided with a Transport menu that facilitates easy access to appropriate design directories and associated applications software.

Accessing and Configuring the design environment is achieved using the "transport" tool. Students should start a UNIX terminal window and invoke the transport tool by typing the command:

- `transport & <RETURN>`

The *Transport* form should appear as shown below.

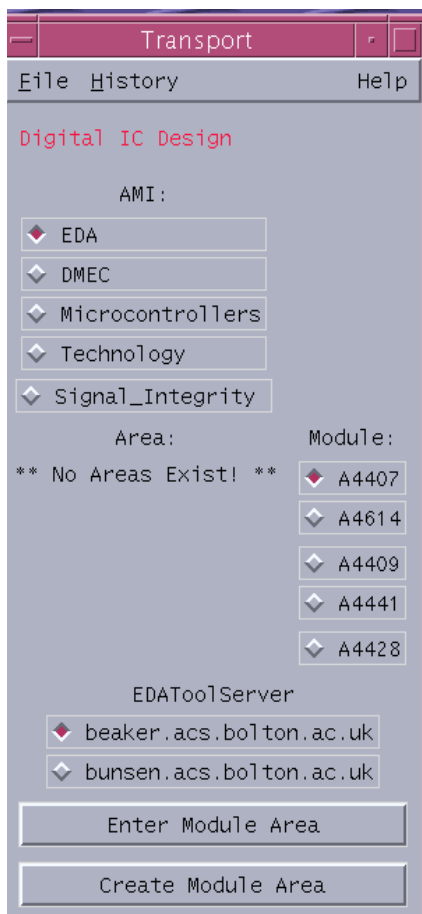


Fig: Transport Menu with no module areas created for A4407

The menu enables a module design area to be created and then entered by specifying the module

being studied. Modules are classified by type and function.

3.1 Using the Transport Form

Click on the **EDA** button to display a list of modules within that classification.

- Select the module **A4407**

If you are using the transport tool for the first time for this module there will be no design areas present and the “Area” field will be blank. In this case you will need to create the default structure by using the “Create Module Area” button.

- Click on the **Create Module Area** button to the design areas.

This may take a few seconds. Once this has run successfully the “Area” field will be populated. As shown in the figure “Transport Menu with module areas specified”.

Now select the Walkthroughs area. Only the *Walkthroughs* area will be used for this exercise.

- Click on the **Walkthroughs** button

The *Transport* menu should now be as shown below.

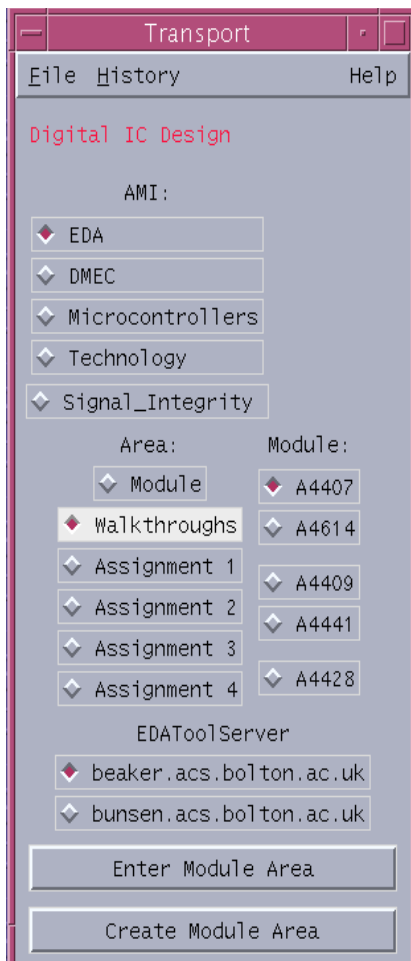


Fig: Transport Menu with module areas specified

Now click on the **Enter Module Area** button to open up a configured UNIX terminal window.

All subsequent commands will be typed in this window. This window will be in the correct location, in this case the “Walkthrough” area. For the 4407 module this will be physically located at “~/AMI/A4407/Walkthroughs”. This area is also configured to allow you to run all the relevant tools and

4 Starting Cadence and the AMS 0.35um Design Kit

In the configured 4407 terminal window you can start the design kit using the UNIX command:

- **amiselect fb <RETURN>**

After a short delay the CADENCE Command Interpreter Window (CIW) as shown below will appear at the bottom of the screen. The window provides a tool bar for the top level menu commands and a display window for status information.

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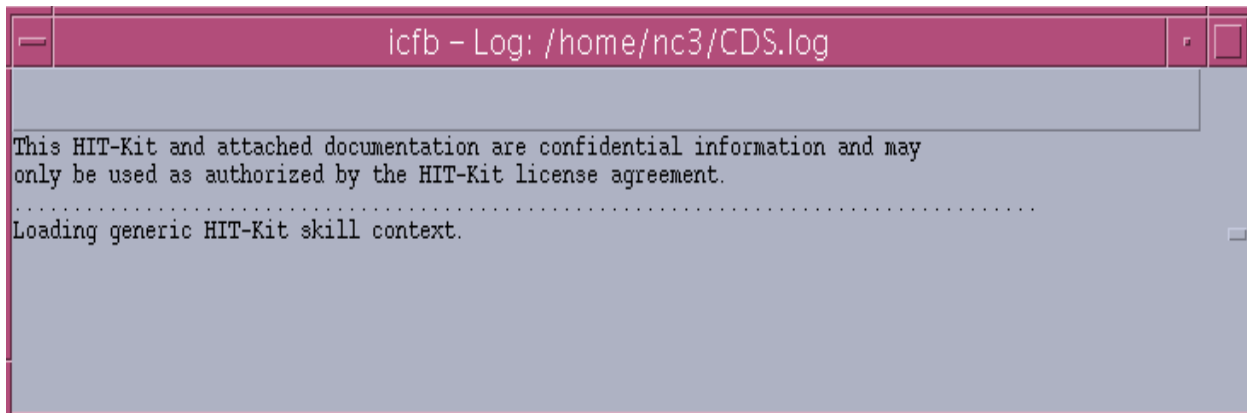


Fig: The CADENCE Command Interpreter Window (CIW)

The Cadence *Library Manager* as shown below will also be displayed.

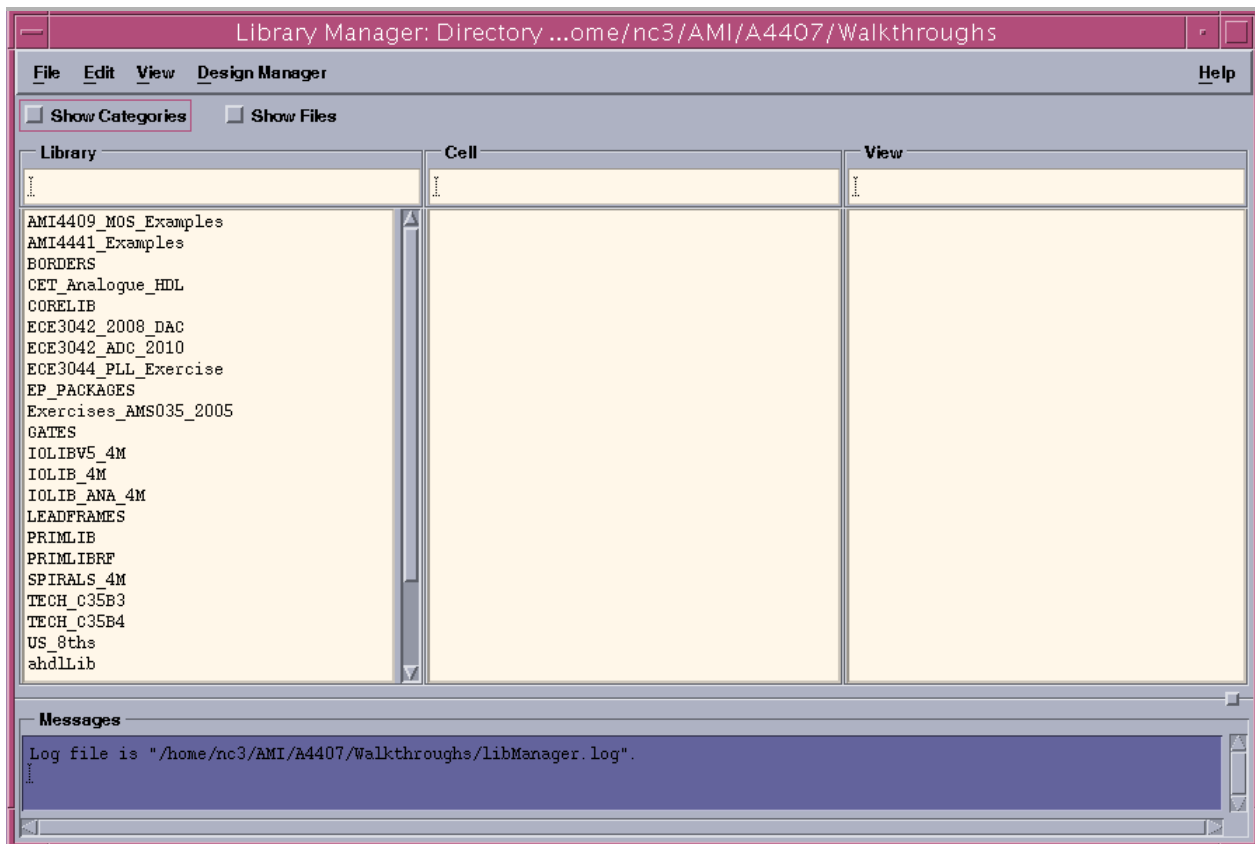


Fig: Library Manager

The *Library Manager* enables design libraries, cells and cell views to be created, opened, copied,

5 SCHEMATIC ENTRY

5.1 Introduction

This section details the operating instructions for invoking CADENCE and running *Composer* to enter the stepper motor driver schematic.

Instructions are provided for entering logic components, input/output pins and wires and for checking and saving the design.

5.2 Creating a schematic cellview called display

Click on the **examples** library in the *Library Manager* and verify that it highlights.

Select **File -> New -> Cellview** from the *Library Manager* to display the *Create New File* form.

Click in the *Library Name* box to display the list of available libraries.
Select **examples** from the list.

Click in the *Cell Name* box and enter **display** as the cell name.

Verify that the *View Name* box has been set to **schematic**.

Verify that the *Tool* box has been set to **Composer -Schematic**.

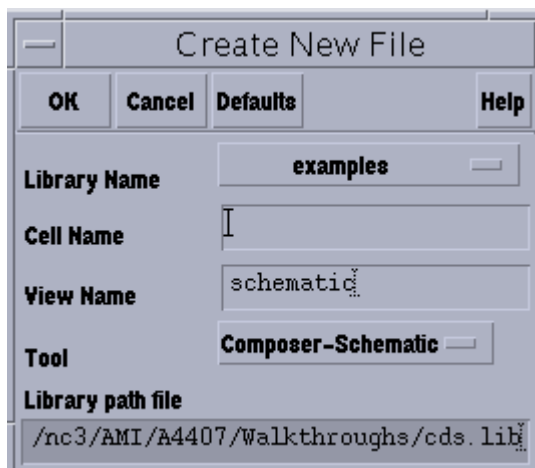


Fig: The Create New File form

Add in the entries for the cell name and accept the form by clicking on **OK**.

A message will appear in the CIW confirming successful creation of the cellview and an empty schematic window will now open.

5.2.1 Supplementary Information

Note: In subsequent sessions should you wish to display or edit the schematic that you are about

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to create you can select it either from the CIW or via the Library manager. The recommendation would be to use the Library manager

From the *Library Manager* select the required *Library Name* (**examples**), *Cell Name* (**test1**) and *Viewname* (**schematic**) as shown below

Select **File - Open** from the *Library Manager* to open the schematic, or right click on the schematic view to bring up the context sensitive options.

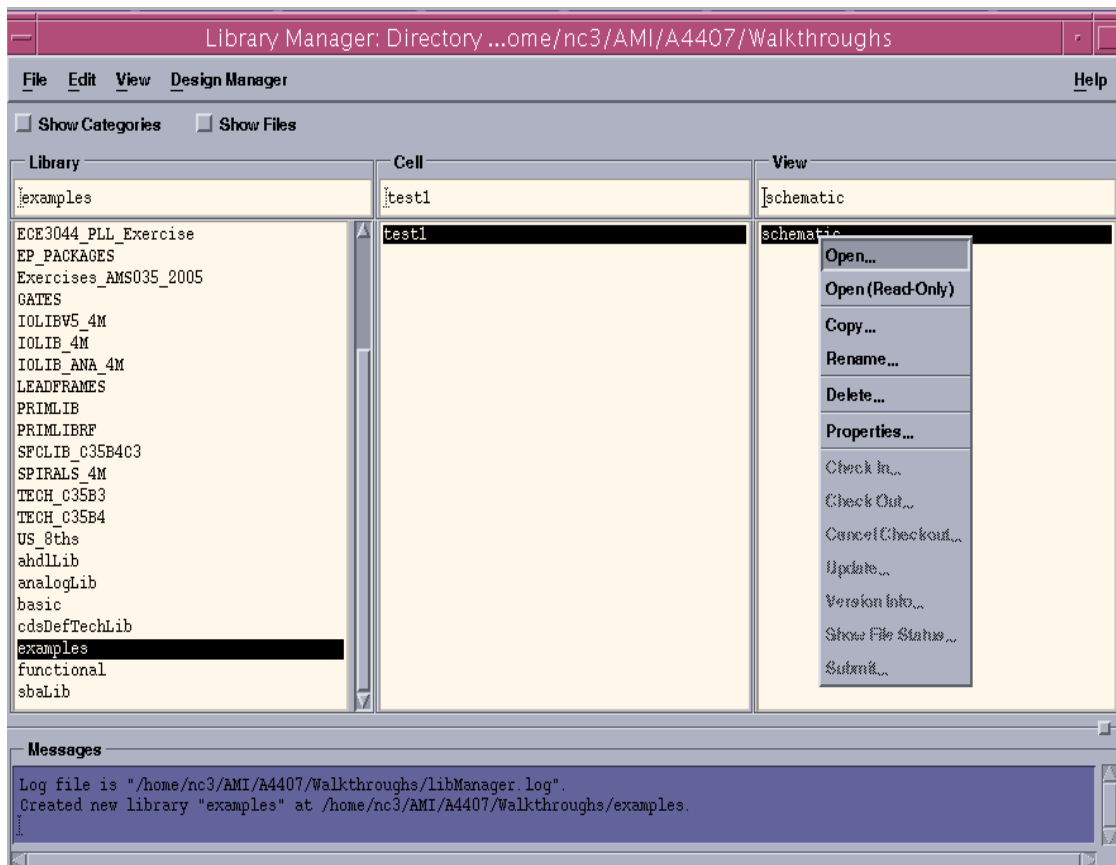


Fig: Selecting the test1 schematic from the library browser

6 Entering the Schematic

The schematic window displays the main options along the top and a subset of these options in icon form down the left hand side.

The circuit schematic shown below will be assembled in three stages:-

1. Enter the logic components
2. Enter the input and output pins

3. Wiring up the logic components and input/output pins

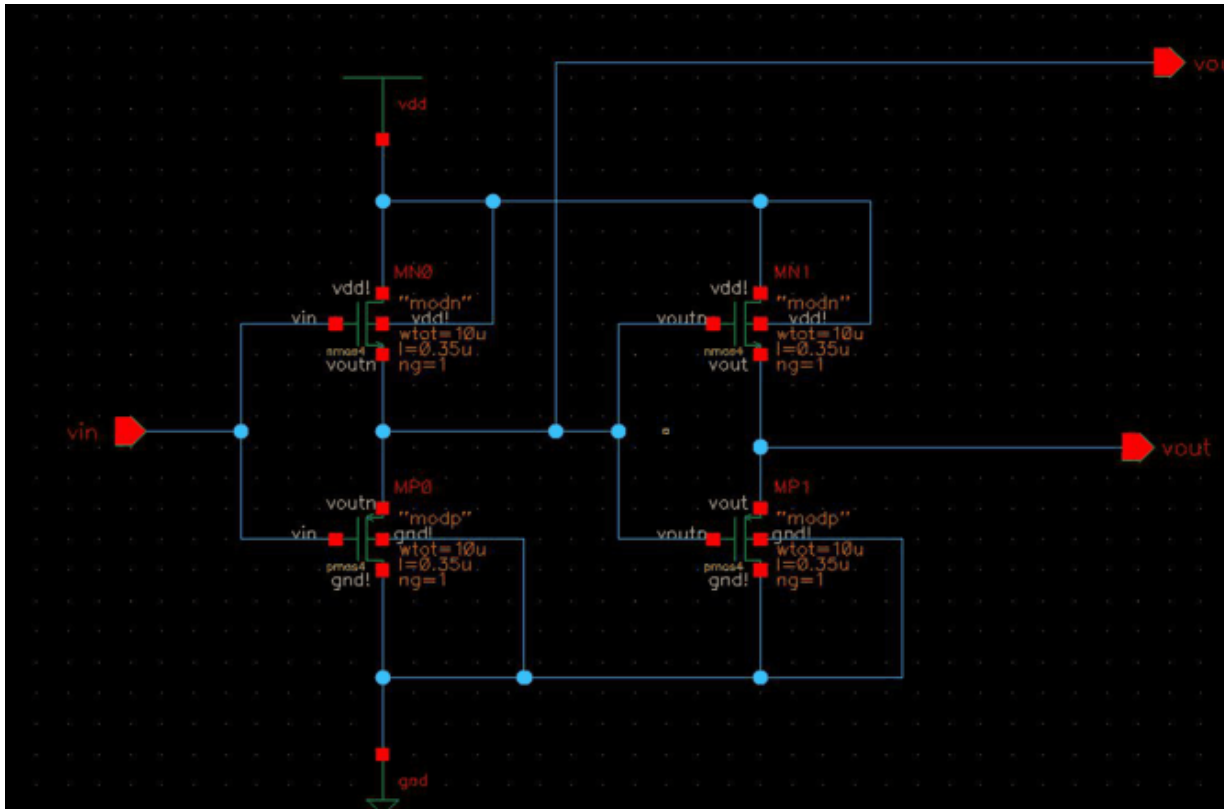


Fig: Final Schematic

6.1 Entering the Logic Components

Select Add - Instance (or use the i key on the keyboard) to display the *Add Instance form* as shown below.

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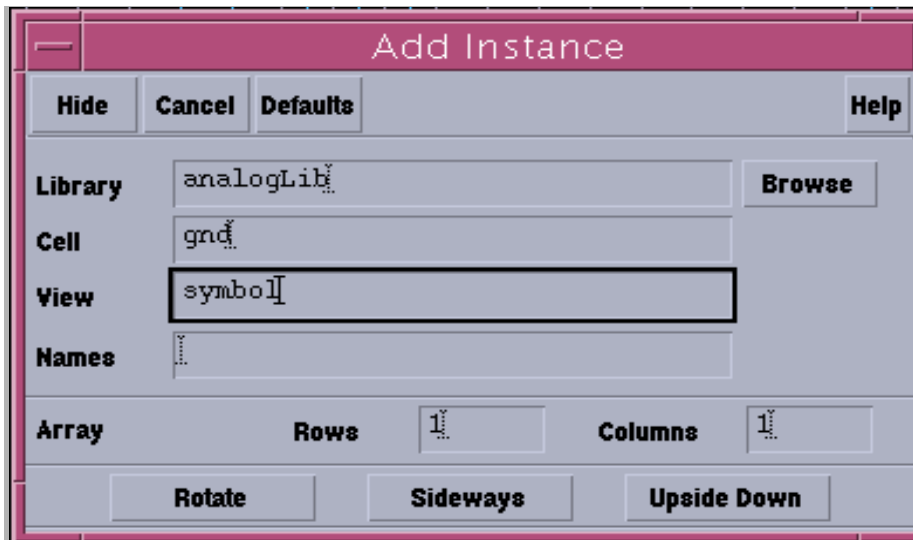
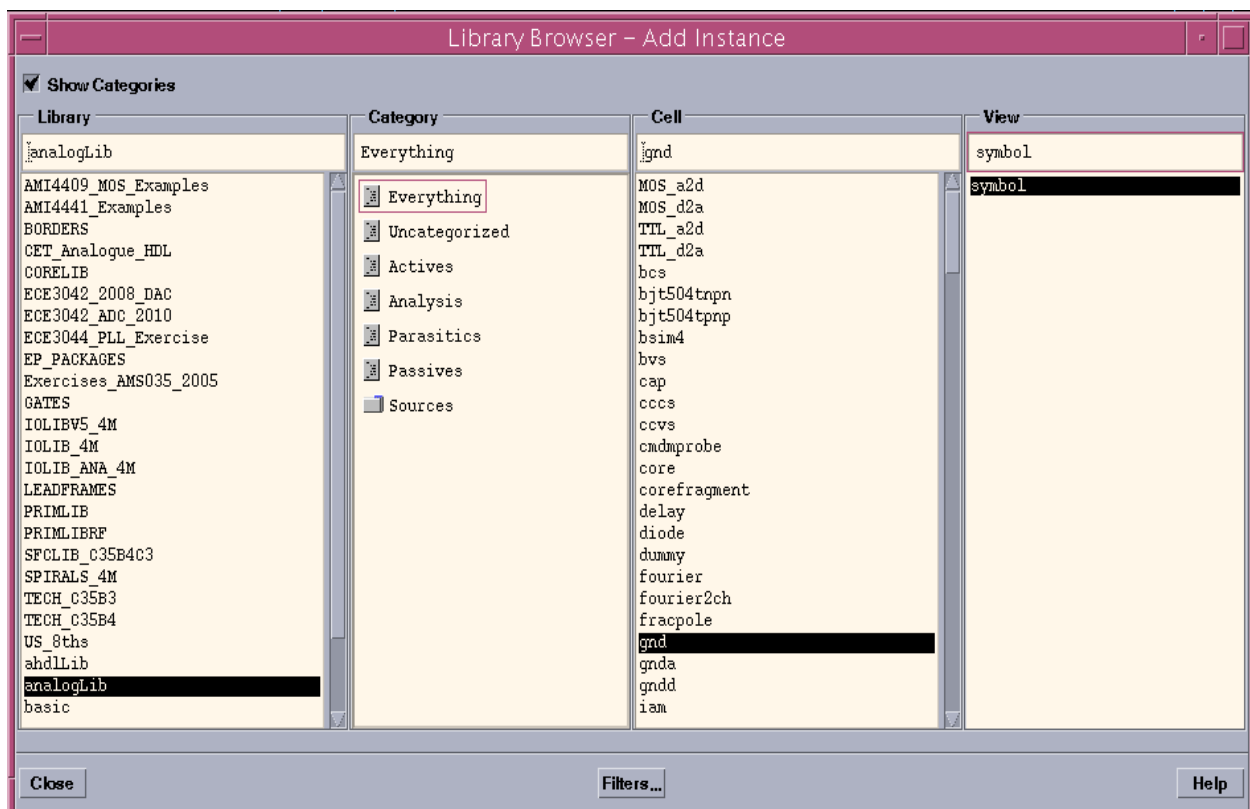


Fig: Add Instance Form

Select the *browse* option to open the “Library Browser - Add Instance” form. This form should resemble the one shown below.

- Hint: Be careful not to confuse this with the normal Library browser form the functions are different.



Note that the “Show Categories” option is on. Indicated by the tick in the top left hand corner.

6.2 Schematic Components

The following components were used to construct the schematic. Please note that schematic pins are not library components and may be added using the Add->Pin or associated icon. Their use will be described later.

Table 2: Schematic Library Components

Library	Name	View to use
analogLib	vdd	symbol
analogLib	gnd	symbol
PRIMLIB	nmosm4	symbol
PRIMLIB	pmosm4	symbol

Use the mouse to navigate “Library Browser - Add Instance” form and select the cell and cell view required.

For example if we selected the PRIMLIB nmosm4

The nmosm4 component will now be attached to the cursor in the schematic window. At this point you may wish to move the *Library Browser* out of the way to facilitate the placement of the component. Simply press and hold down the left hand mouse button in the window title bar and drag to the required location.

Now position the component where required in the schematic window and click the left hand mouse button to place and instance in the required location.

Press the <ESCAPE> key to terminate the Add Instance option and release the component from the cursor. In fact the majority of operations can be terminated using the <ESCAPE> key.

Hint: If you are unsure of the selected function look at the base of the schematic window. The function of the left, middle and right mouse buttons is shown.



Fig: Example of Mouse Functions at Base of Schematic Window

6.2.1 Supplementary Information

6.2.1.1 F3 accessing the Options form for the selected command

Many commands have additional options place instance, copy and move amongst them. These additional options form can be called up using the F3 button. This also allows you to hide the additional options form as well.

6.2.1.2 Zoom In/Out/Fit

There are a number of zoom options available by bindkeys of via the Window->Zoom option

Table 3: Useful Zoom options

Menu	Bindkey	Function
Window->Fit	f	Fit
Window -> Zoom in by 2]	Zoom in X2
Window -> Zoom out by 2	[Zoom out X2
Windows Redraw	F6	Refresh Window
Scroll View Left/Right	CursorKey Left / Right	
Scroll View Up/Down	Cursor key Up/Down	

6.3 Creating the schematic

It may also be necessary to zoom out/in the display before placing further components. Select Window - Zoom Out By 2 from the schematic window menu repeatedly until the required display size is achieved.

You may wish to use the keys fit, “[“and “]” to zoom in and out to make the work easier.

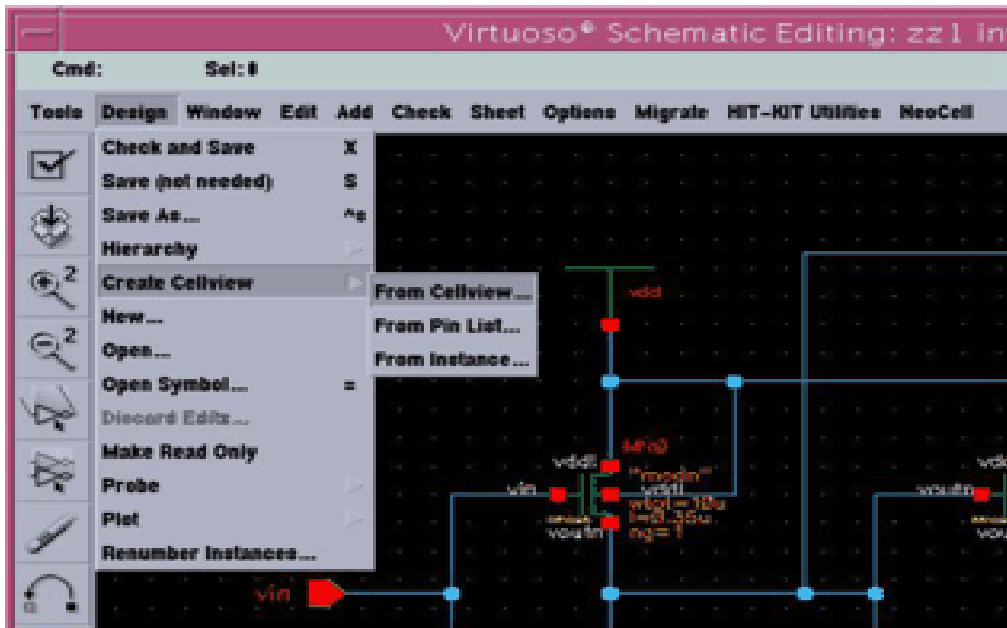
Place another instances of the nmos4 and two pmosm4 as shown in the schematic.

This can be done in any of the following ways:-

Repeat the Add Instance procedure as detailed above for each required instance

The schematic should resemble that shown below

Fig: Figure 8 The Schematic



6.4 Entering the Input/Output Pins

The input and output pins are defined as follows:-

Signal Name	Type	Function
vin	input	driver reset

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vout	output	non inverted buffered output
voutn	output	inverted buffered output

Zoom into the area surrounding the XNR20 gate in the top left hand side of the schematic by selecting Window - Zoom In (or the z key). Position the cursor at the top left of the zoom area and press and hold the left hand mouse button. Drag the cursor to the bottom right of the zoom area and release the mouse button. The selected area will now be enlarged.

At any time you can revert to the full window view by selecting Window -> Fit (or the f bindkey).

Now select Add -> Pin (or the p bindkey) to display the Add Pin form as shown below.

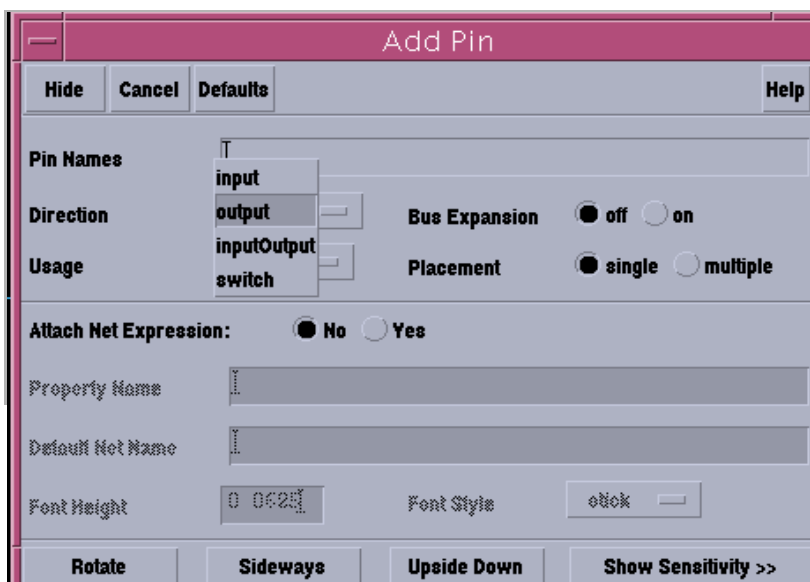


Fig: Figure 9 The Add Pin Form

6.4.1 Entering the inputs pins

Make sure the direction field of the form is set to input

Select the form and add either one or all of the input pin names into the box, separated by spaces. If using multiple pins then one mouse click will place one pin.

Enter the pin name "vin" into the Pin Names box and terminate the input by pressing the RETURN key. An input pin symbol will now be attached to the cursor. Locate the pin as detailed in the circuit diagram at the beginning of the walkthrough and click to fix in position. Check that the pin name is displayed adjacent to the pin as shown below.

6.4.2 Entering the output pins

Note: Input/Output pins can be deleted and moved using the same procedure as for components. Follow the same procedure for the output pins referring to the circuit diagram. (Make sure the direction field is set to output before placing the pins.

6.5

Repositioning and tidying up the schematic

At this stage you may want to reposition some or all of the components. Given the potential run of the wiring interconnects required. This is most easily accomplished by using the group move facility.

6.6 Wiring the Components

There are two methods of connecting components depending on their relative positions.

6.6.1 Automatic Connection

The connection between the input pin reset and the inverter is an example.

Select Add - Wire (narrow) or the w key.

Click on the input pin named reset to define the wire source. The wire will now be attached to the cursor. Click on the input terminal of the inverter to establish the wire destination and the wire will now be connected.

6.6.2 Manual Connection

This allows you decide on the location of the “corners” for the wires.

Click on the output terminal of the inverter and guide the wire by clicking on each required horizontal/vertical turning point until the wire destination is reached.

Repeat for the remainder of the wires as detailed in the circuit diagram

Cancel the Add Wire operation when you have completed all the connections by pressing the <ESC> key.

6.7 Checking and Saving the Design

When complete the schematic should resemble the one shown in the figure Final Schematic

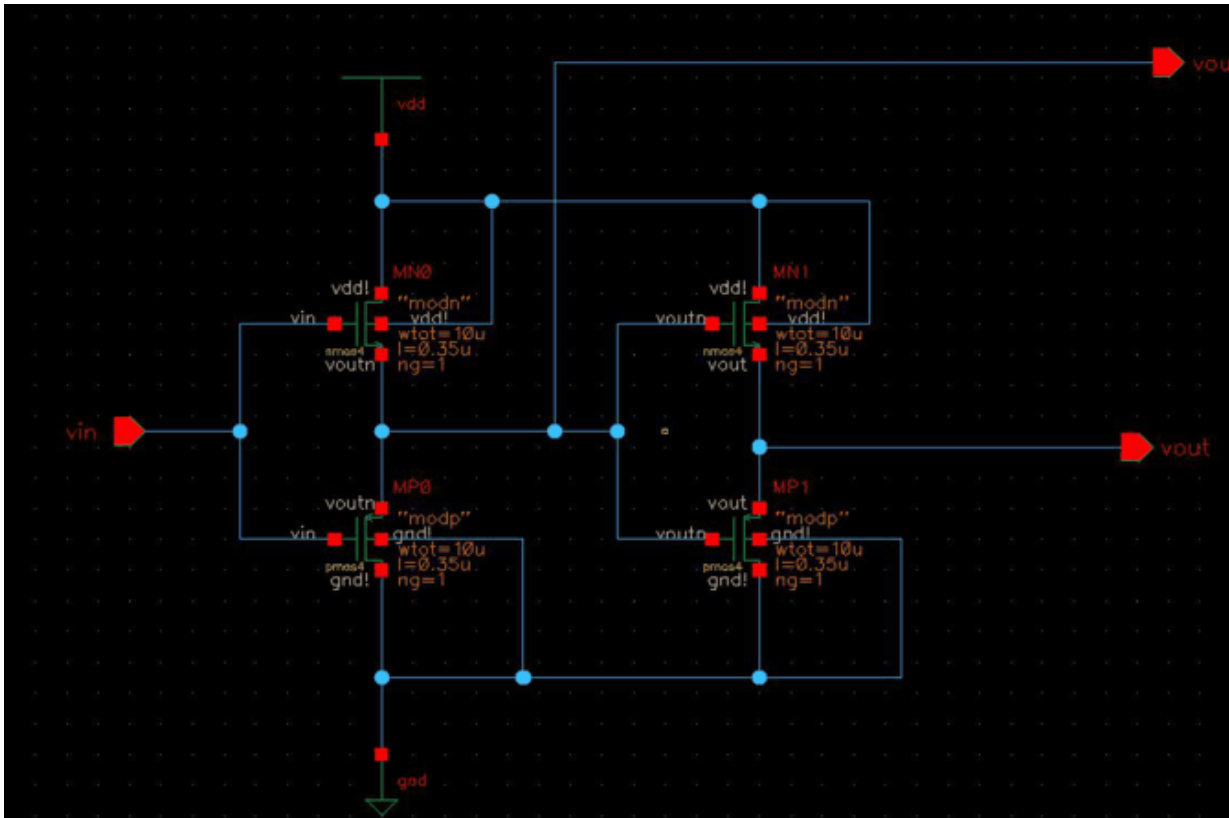


Fig: Final Schematic

The design must be checked for schematic errors before saving in the database.

Select Design - Check and Save (or the X key).

Inspect the CIW for any errors and warnings that may have been reported. Expect four warnings relating to the unconnected inverse outputs of the flip-flops. These will flash on the schematic but can safely be ignored.

Errors however must be corrected. As for warnings the offending components or wires will be highlighted on the schematic for reference. Correct the errors and repeat the Check and Save operation until the schematic is error free.

Hint: The most common error is usually to not fully connect to a pin. Leaving a small gap between the wire and the pin.

Hint: You can use the Check -> Find Marker form to zoom between the errors on your schematic. The CIW will list the errors, and it a yellow blinking box will surround the error on the schematic. However on larger schematics this can be a tad small and in this case the Check -> Find Marker tool is used. Select the "Zoom to Markers" option and control the zoom size to make life easier.

Hint: You will notice I have avoided making any 4 way interconnects (cross roads). This is because the Cadence tools, in order to avoid potential issues will flag such connections as a warning. The reason is that a "+" could either be a cross over of a 4 way connection. Accidents do happen and the Cadence tools endeavour to minimise those issues. Hence I only ever use "T" connections. It is not a problem just minimising the number of warnings a schematic will issue.

7 Creating a symbol and test bench

7.1 Introduction

This section details instructions to simulate the design above.

We are going to use the Spectre Analogue simulation tools for this exercise.

Whilst it is possible to use file driven batch mode simulations it is usual, for smaller simulations to use test schematics and the range of spice instruments and functions available in all analogue simulators. To this end as we do not wish to have any elements other than those required for the design on the schematic. We will create a symbol for the schematic. This will be then used on test schematics and in our design. This is standard practice in that no elements not explicitly destined for the final design should be present. The one exception would be items such as the information frame, which are automatically discarded.

Instructions are provided to create a testfixture file for the simulation test vectors, run the Verilog simulator and display graphically the output results.

Creating the Symbol

Once the schematic has no errors we can create the symbol. This also creates additional information that supports the simulations and layout tools.

From the Schematic Design tool select the Design -> Create Cell View -> From CellView command to open up the create cellview form.

- Design -> Create Cell View -> From CellView

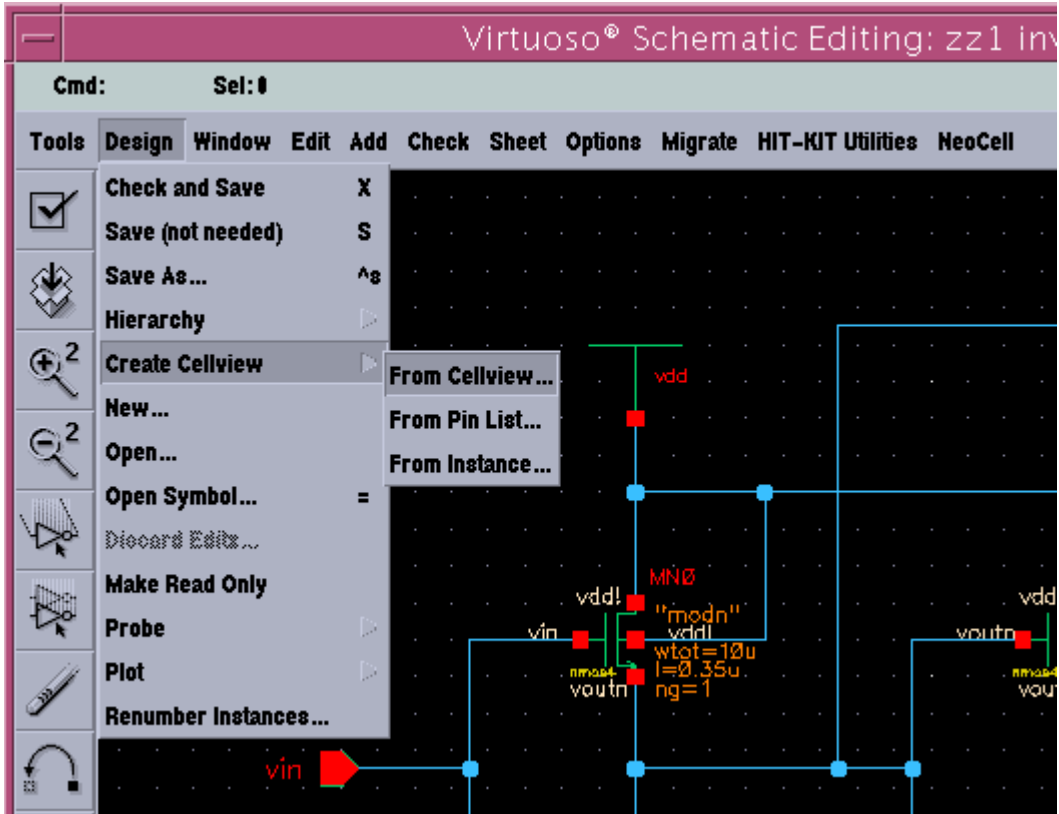


Fig: Create Cell View From Cell View Menu

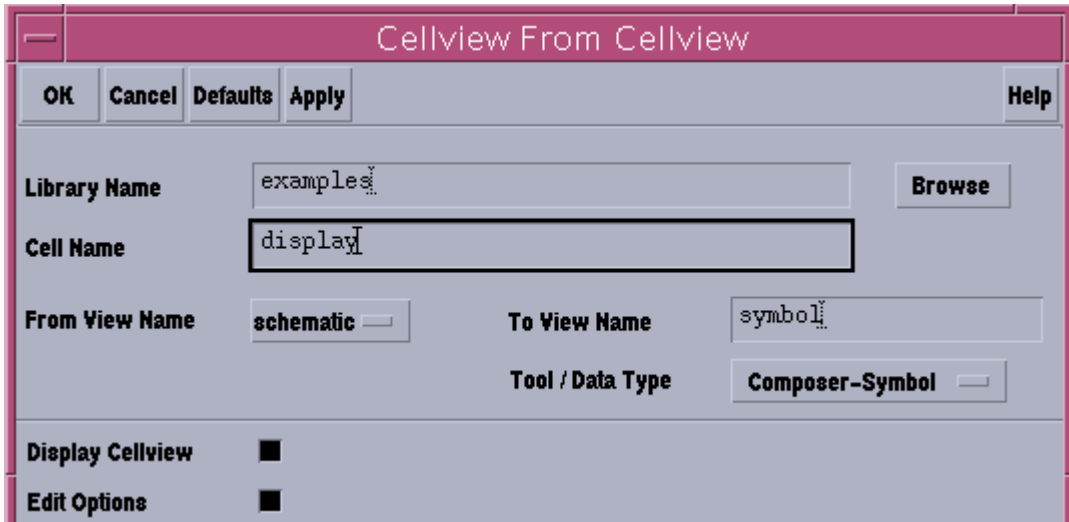


Fig: Create CellView from CellView form

The default settings are fine in this situation. Now Select the “OK” from this form to display the Symbol Generation Options form.

- “OK” the form

The image shows a dialog box titled "Symbol Generation Options". At the top, there are buttons for "OK", "Cancel", "Apply", and "Help". Below these are three text input fields: "Library Name" containing "examples", "Cell Name" containing "display", and "View Name" containing "symbol". The main section is titled "Pin Specifications" and contains four rows, each with a text input field and a "List" button. The rows are: "Left Pins" with "vin", "Right Pins" with "vout voutn", "Top Pins" (empty), and "Bottom Pins" (empty). Below this is a section titled "Exclude Inherited Connection Pins:" with three radio buttons: "None" (selected), "All", and "Only these:". At the bottom of the dialog are four checkboxes: "Load/Save", "Edit Attributes", "Edit Labels", and "Edit Properties", all of which are currently unchecked.

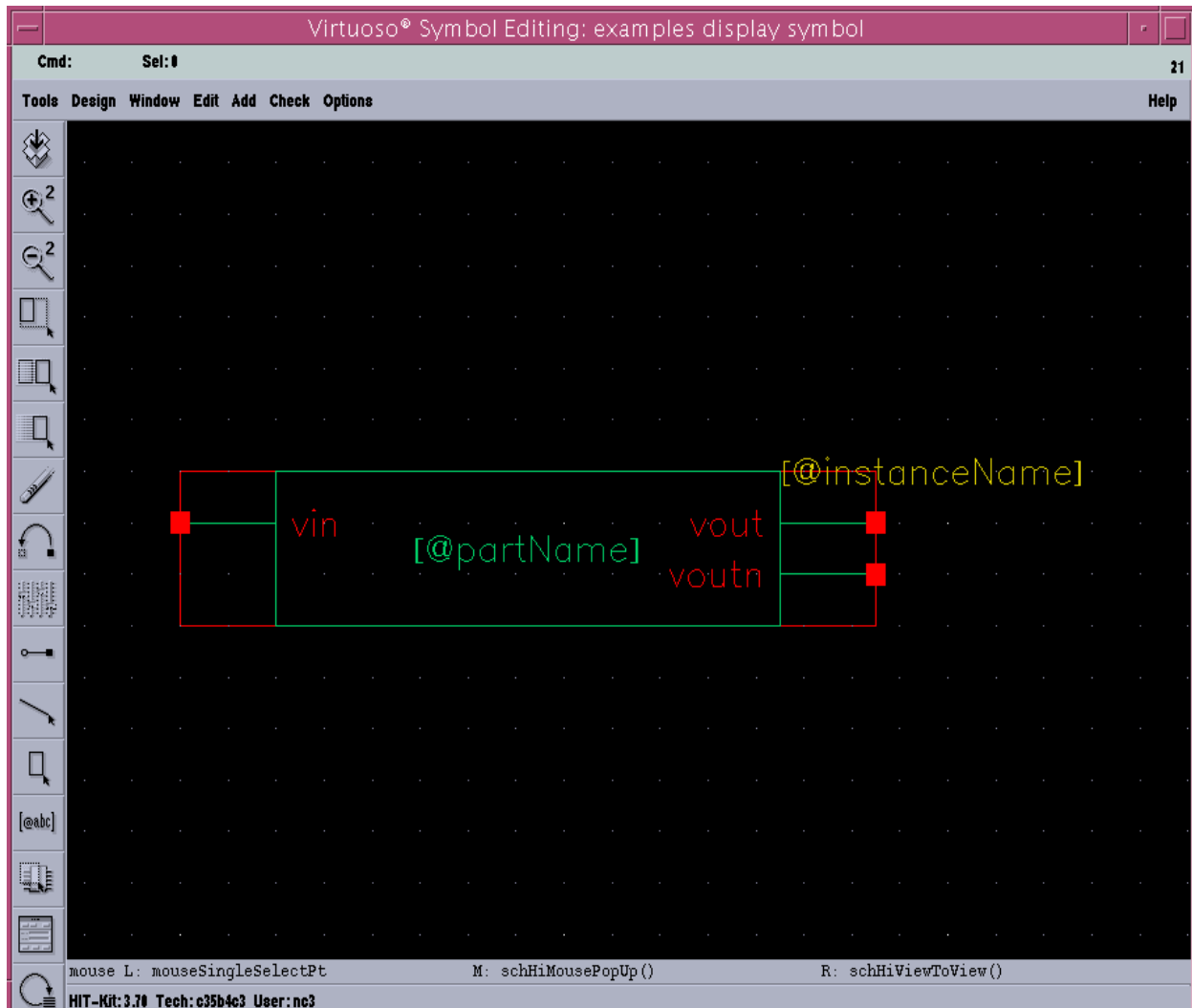
Fig: Symbol Generation Options Form

Again the default values are fine in this situation, "OK" the form to create the symbol.

- "OK" the form.

This will open up the Virtuoso Symbol Editing Form. Displaying the finished symbol. Select the Design -> Check and Save options on this window then close the window using the Window -> Close option.

- Design -> Check and Save
- Window -> Close



7.2 Creating the Simulation Test Schematic

We now need to create a new schematic as our test schematic. Use the Library Browser or the CIW File -> New CellView option to invoke the Create New File from.

Using the "Library Name" cyclic field select the examples library. Use a "Cell Name" of Test_display_1 and a "View Name" of schematic. The tool setting should be the default "Composer_Schematic"

- Library Name : examples
- Cell Name : test_display_1
- Cell View : schematic
- Tool : Composet-Schematic

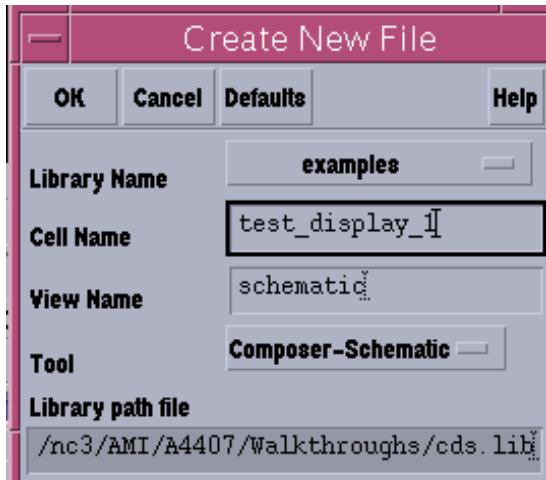


Fig: Create New File Form

This will create and display the schematic “test_display_1”.

7.3 Editing the schematic

We now need to place the following components on the schematic

Table 4: Schematic Library Components

Library	Name	View to use
examples	display	symbol
analogLib	gnd	symbol
analogLib	vdd	symbol
analogLib	vdc	symbol
analogLib	vpulse	symbol

7.3.1 We will also need to place two schematic output pins. I have called my top_vout and top_vountrn.

7.3.2 Placing the vdc

When placing the vdc the placement form should be use to set the "DC Voltage" to 5 volts. If you miss this state see the section 7.4 “Changing properties on placed instances.

Apply To

Show system user CDF

Property	Value	Display
Library Name	analogLib	off <input type="checkbox"/>
Cell Name	vdd	off <input type="checkbox"/>
View Name	symbol	off <input type="checkbox"/>
Instance Name	V	off <input type="checkbox"/>

User Property	Master Value	Local Value	Display
Ivsignore	TRUE		off <input type="checkbox"/>

CDF Parameter	Value	Display
AC magnitude		off <input type="checkbox"/>
AC phase		off <input type="checkbox"/>
DC voltage	5 V	off <input type="checkbox"/>
Noise file name		off <input type="checkbox"/>
Number of noise/freq pairs	0	off <input type="checkbox"/>
XF magnitude		off <input type="checkbox"/>
PAC magnitude		off <input type="checkbox"/>
PAC phase		off <input type="checkbox"/>
Temperature coefficient 1		off <input type="checkbox"/>
Temperature coefficient 2		off <input type="checkbox"/>
Nominal temperature		off <input type="checkbox"/>

Fig: Filled in VDC form

7.3.3 Placing the VPulse

When placing the vpulse we need to set a number of parameters. These are:

Table 5: Vpulse Settings

Parameter	Value
DC Voltage	0
Voltage 1	0
Voltage 2	0
Delay time	0
Rise time	1n
Fall time	1n
Pulse Width	100n
Period	200n

A correctly filled in form will resemble the one shown below

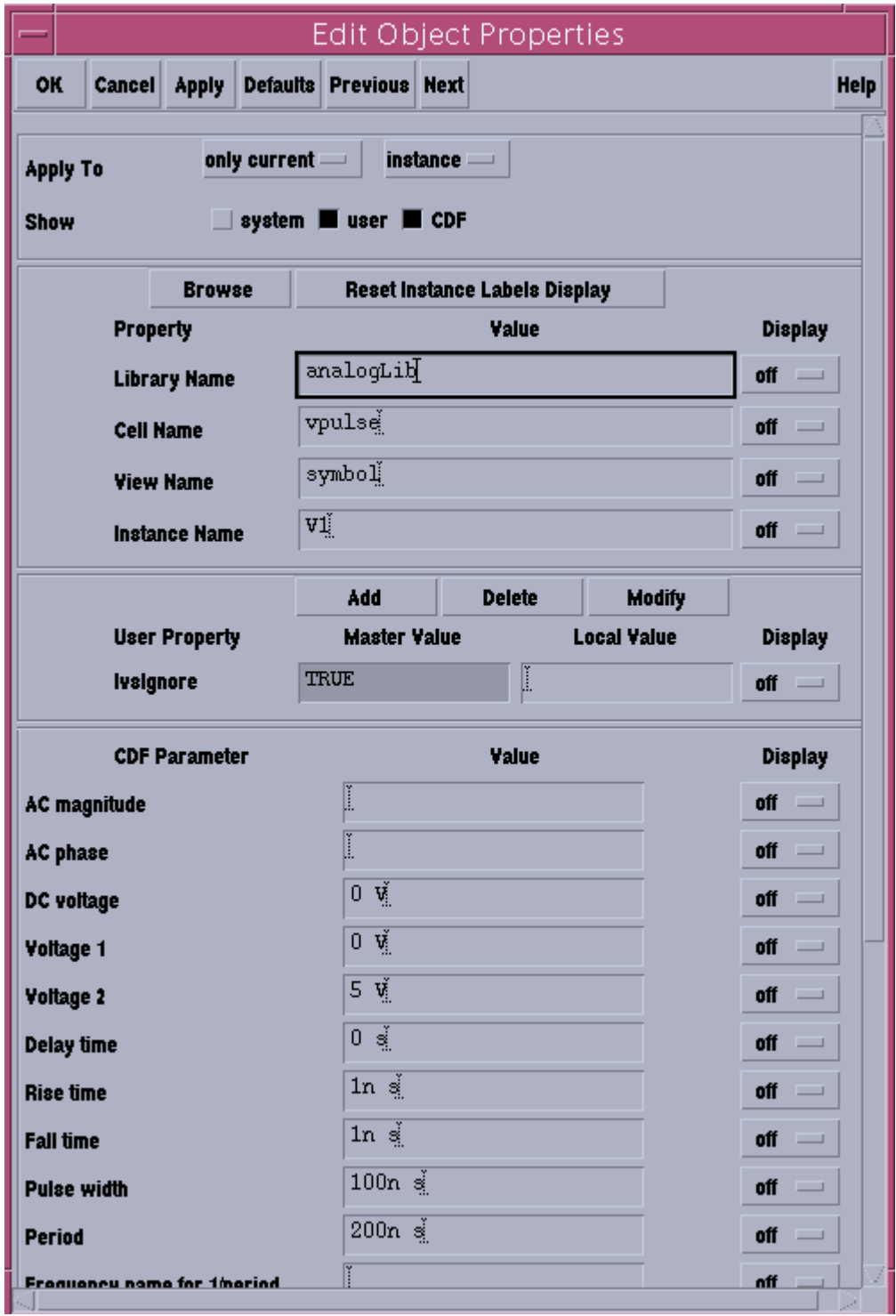


Fig: Filled in vpulse form

- Hint: Cadence can recognise standard extensions when used hence you can enter 1e-9 or 1n
- Hint When entering values in fields with a defined scalar i.e. voltage or time. Cadence will

automatically add an appropriate suffix i.e. S or V, separated from the value entered. Do not confuse the issue by adding your own s or n. This will result in design variables being created and problems with the simulation. This will need to be corrected before continuing. For example the netlister will see 5V or 100ns as using design variables of type “V” or “ns” respectively.

7.4 Finished Test Schematic

The finished schematic in structure and connectivity should resemble the one below.

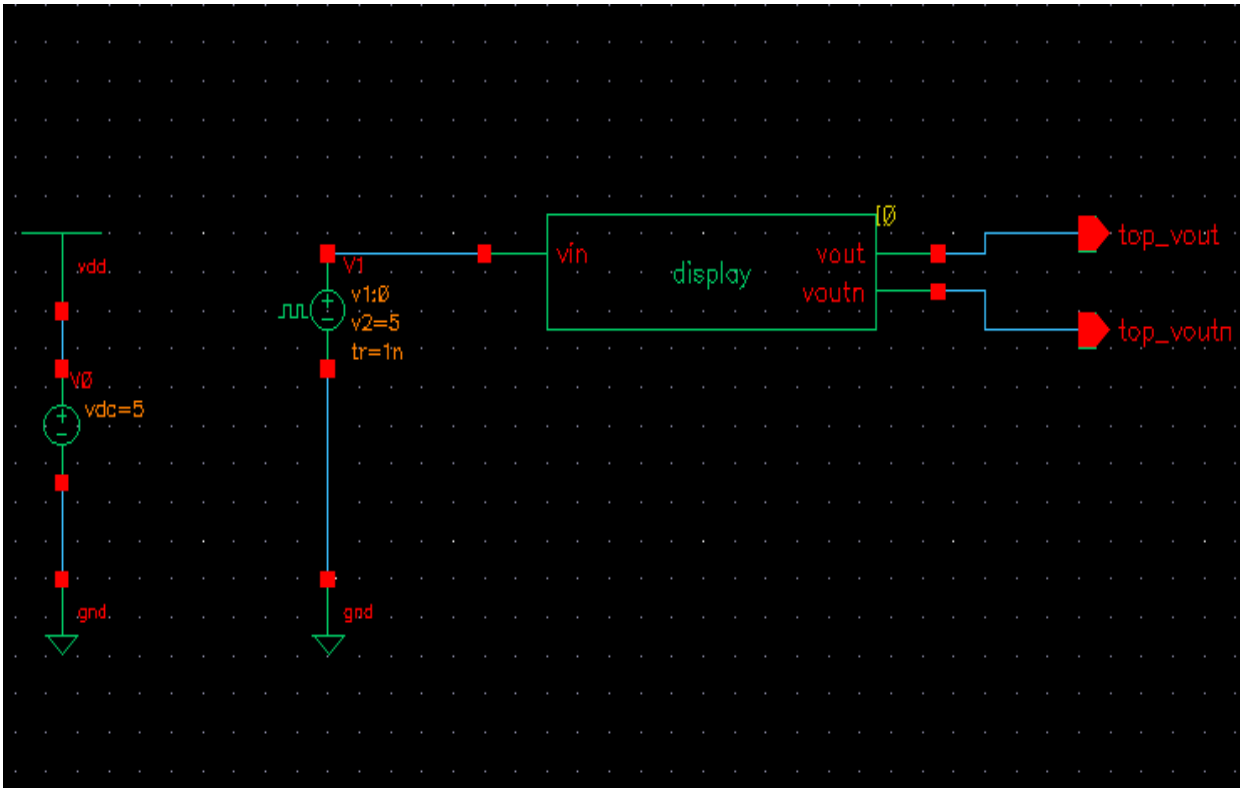


Fig: Final Schematic

Now run a final check and save and ensure there are outstanding warnings or problems. If the schematic passes then we are ready to start simulation.

7.5 Changing properties on placed instances.

Select the instance, by moving the mouse cursor over the instance and left clicking. When selected the item should be surrounded by a white box. The bounding box. By selecting the Edit - Properties, bindkey q or the properties icon we can display and change the properties of this item.

8 Simulation

This exercise will do a basic transient simulation on the schematic created.

8.1 Starting the Simulator

We invoke the simulation environment from the schematic window of the “test_display_1” schematic using the menu option Tools -> Analogue Environment. This will open the Virtuoso Analogue Simulation Environment Tool box.

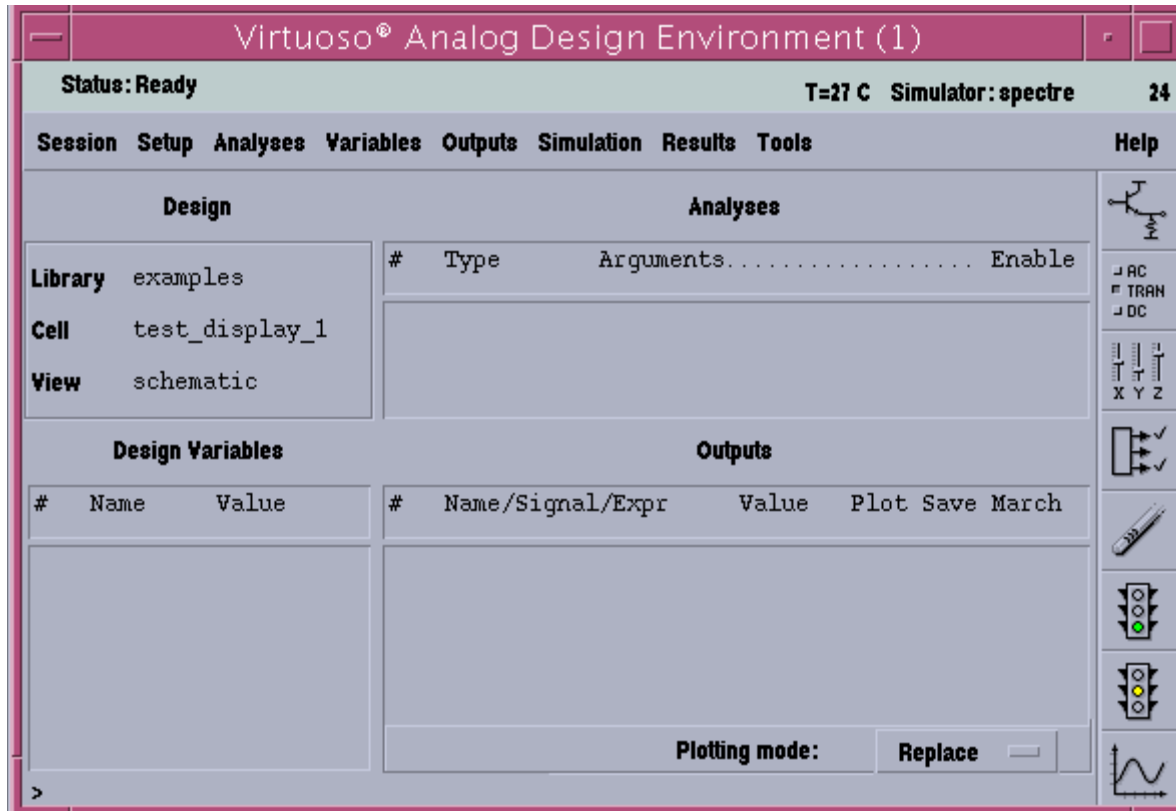


Fig: Virtuoso Analog Simulation Environment

Select Analyses - Choose (or the AC TRAN DC icon second down from the top) to display the *Choosing Analysis Simulation* form.

Verify that the tran button is selected. Click in the Stop Time box and enter 250n. This defines a transient analysis from 0 to 200 nano seconds

The form should be as shown below

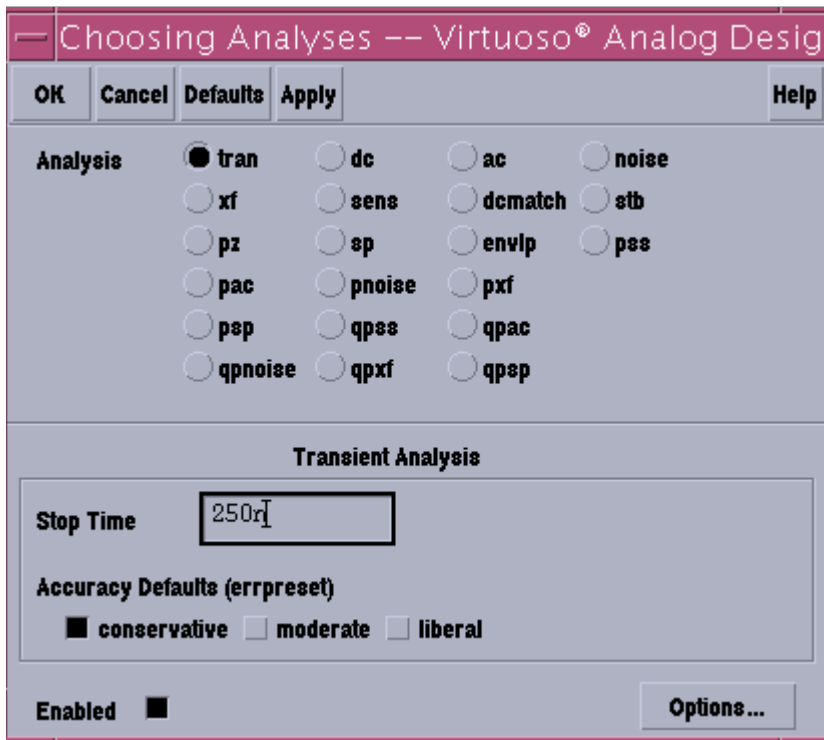


Fig: Analyses Form

Select OK and check that the parameter has been entered into the Analyses section of the *Virtuoso Analog Design Environment* form as shown below

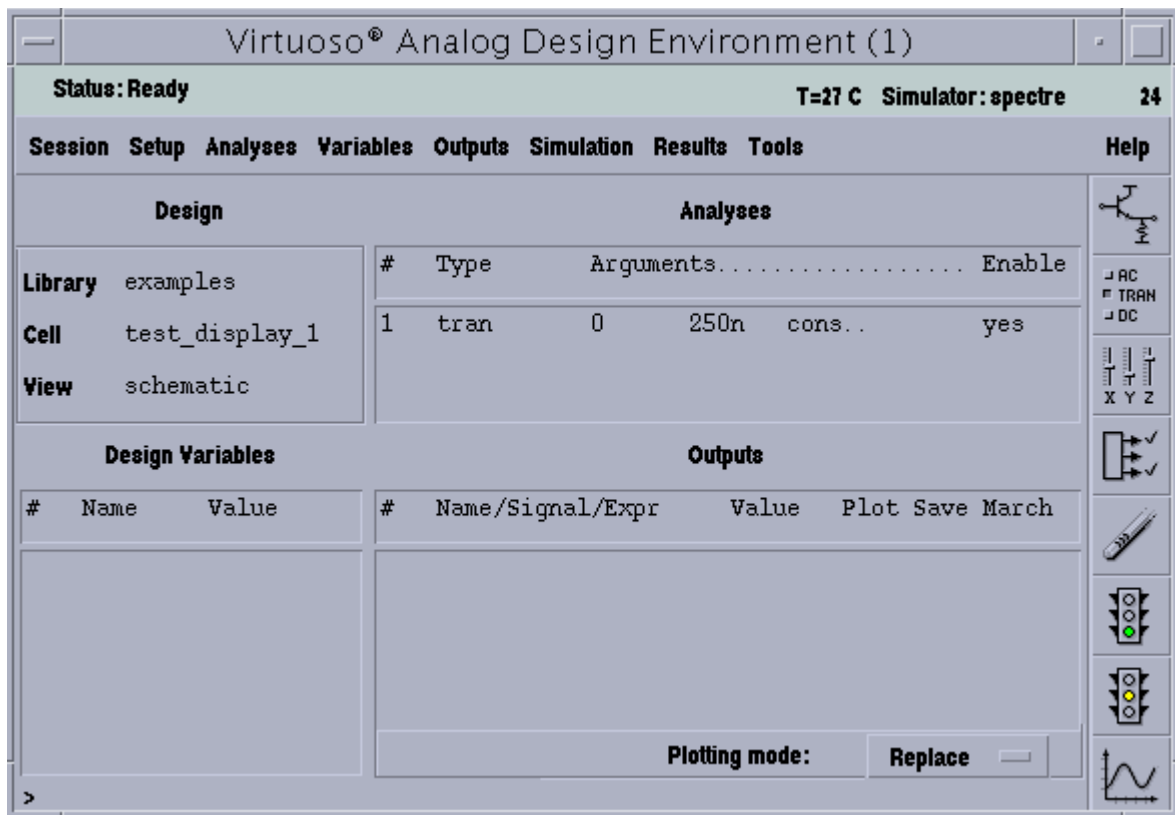


Fig: Simulation form with Simulation Analyses information entered

8.1.1 Running the simulation

Now Select Simulation -> Netlist and Run (or the "green" traffic light icon)

- Simulation -> Netlist and Run

Observe the CIW for status information relating to the production and compilation of the circuit netlist and the running of the simulation. Any errors produced must be corrected and are likely to relate to incorrectly specified components, connections or properties associated with the power supply and input signal sources on the schematic.

8.2 Displaying Results

Select Results -> Direct Plot -> Transient Signal from the *Virtuoso Analog Design Environment* form.

After a short while a blank waveform window will open and the schematic window will be displayed . The bottom trace of the schematic window will display the following prompt.

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```
mouse L: schSingleSelectPt() neoCellSelCh() M: schHiMousePopUp() R:sevl
HIT-Kit: 3.70 Tech: c35b4c3 User: nc3 Select nodes or terminals, press <esc> to finish selection
```

Signals are displayed in the waveform window by selecting their wires in the schematic . Once correctly selected a wire will change colour to match the colour that will be shown in the display.

Click on the input wire, vin, the top_vout and top_voutn wires on the schematic and verify that they highlight in different colours .

Press the <ESC> key to stop select and plot the selected signals in the waveform window as shown below :

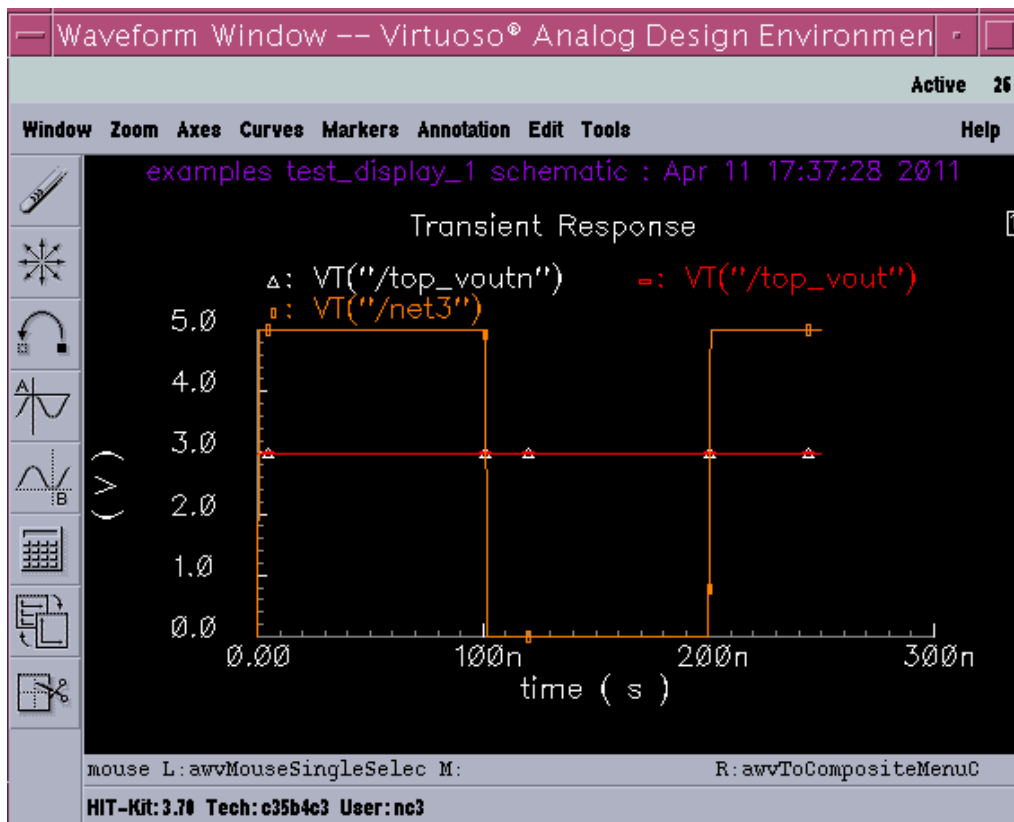


Fig: Waveform window with Axes -> Composite

On the waveform window Select Axes - To convert the display from composite to strip. The waveform window will display the signals individually as below:

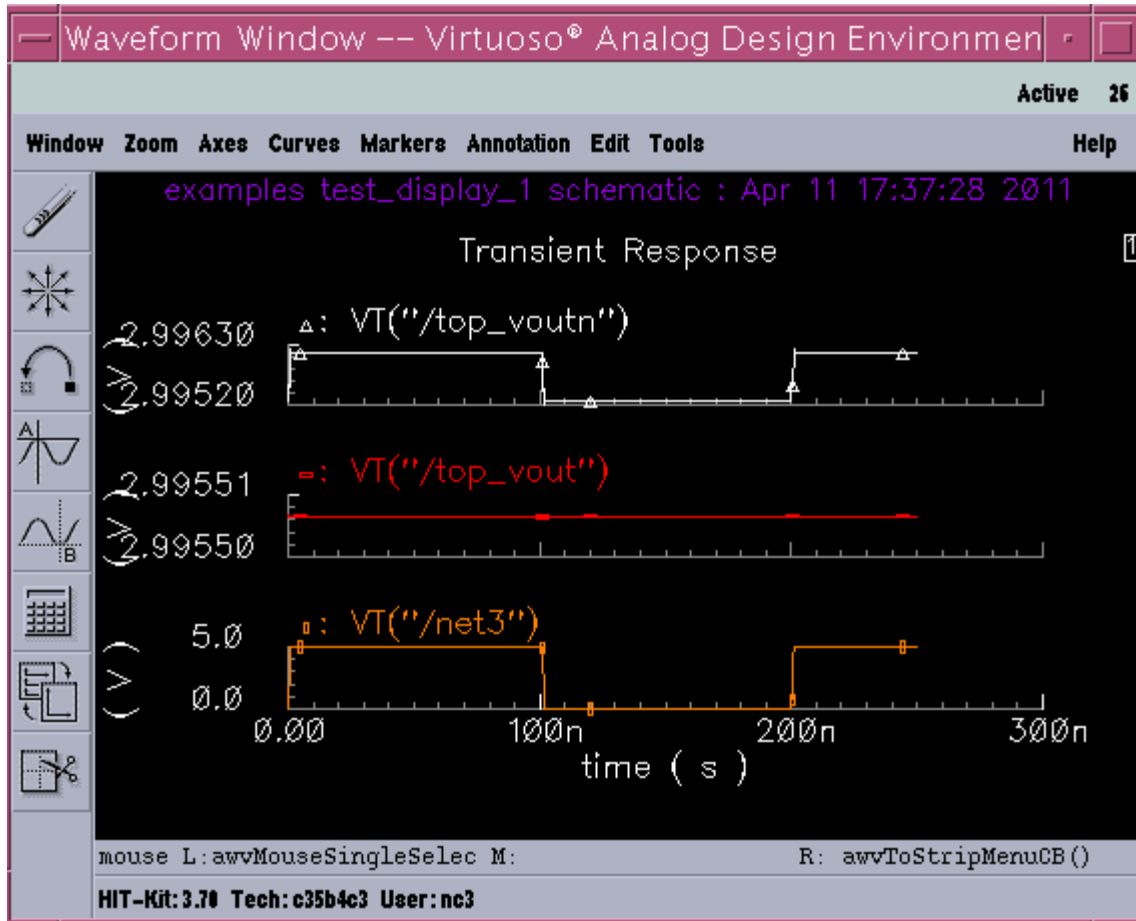


Fig: Waveform with Axes -> Strip Option

Verify that the circuit is functioning correctly

Select Window - Close to close the waveform window

Select Window - Close to close the schematic window

Select Session - Quit to close the Analog Artist Simulation form

In response to the message “Do you wish to save the current state?” select Yes if you wish to save the transient analysis parameters and the waveforms or No if you don't.

8.3 Caveats

It should be obvious that we have skated past a tremendous amount of the functionality and requirements to do detailed analogue design. The situation becomes even more lop sided when one enters the realm of full custom layout. We are not covering at all design methodologies, layout rules or all the other minutiae that are absolutely vital to producing a viable, efficient and professional analogue design.

9 Digital Simulation

9.1 Creating a functional Verilog Model of the design

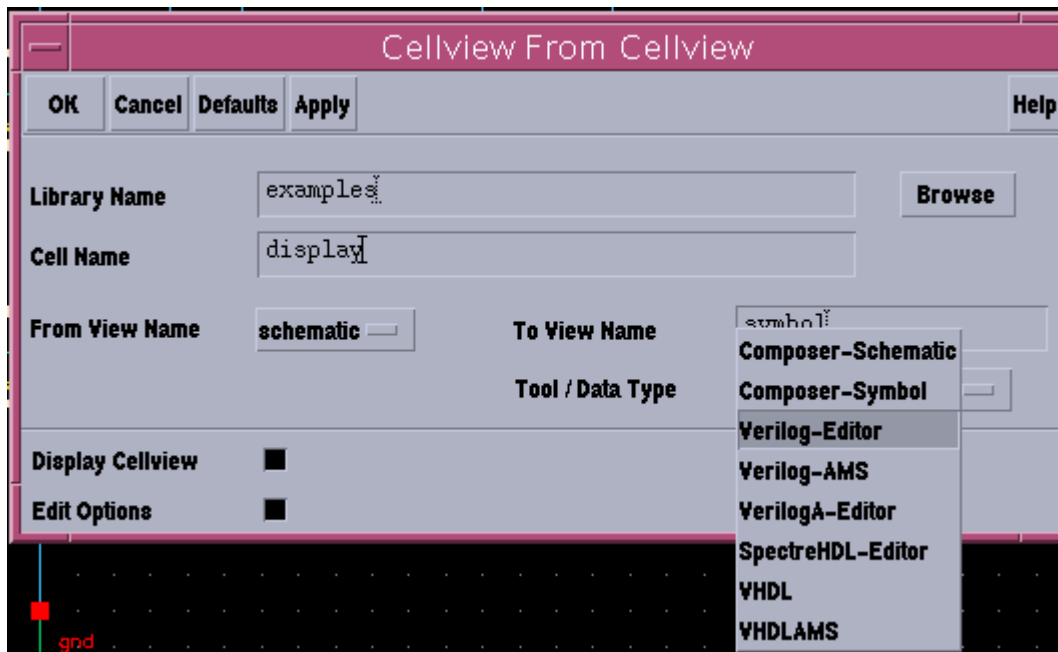
As it currently stands there is no digital model for this circuit. In this exercise we will be creating a functional model, integrated with the analogue, and eventually the layout version of the design. To do this we once again use the Schematic Create Cellview command.

Open up the “display” schematic one using the library browser.

Select the Design -> Create Cellview From CellView menu option to display the Create CellView from.

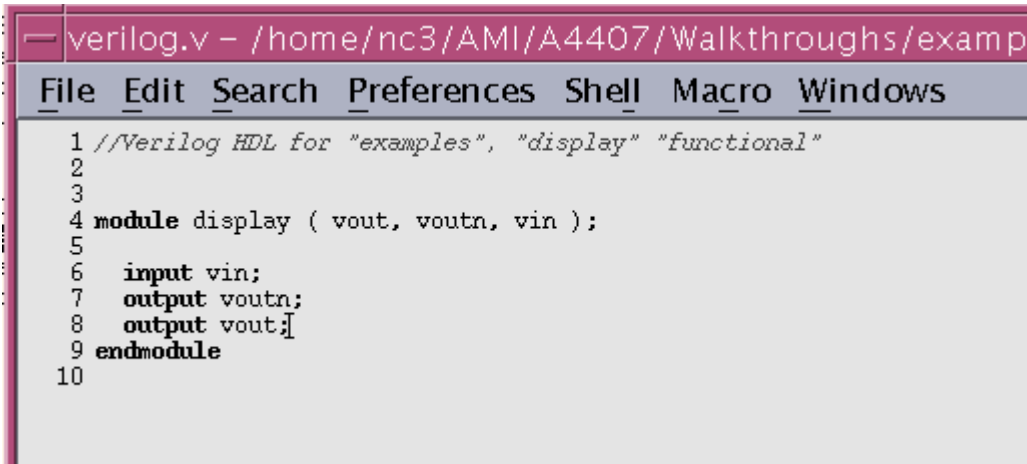
When the form is display select the “Tool / Data Type” to be “Verilog-Editor. Then OK the form.

- Select Tool / Data Type Verilog Editor
- OK Form
- This will create and open for edit a default “functional” view.



Create CellView From CellView form with “Tool / Data Type” “Verilog-Editor Selected”

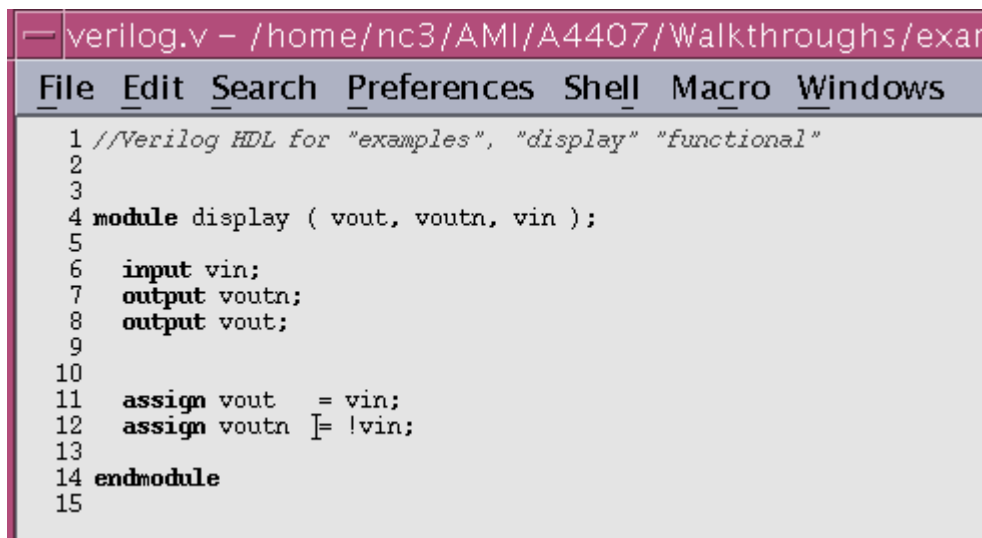
This will open up an edit window with the basic structure and the ports already defined.



```
verilog.v - /home/nc3/AMI/A4407/Walkthroughs/examp
File Edit Search Preferences Shell Macro Windows
1 //Verilog HDL for "examples", "display" "functional"
2
3
4 module display ( vout, voutn, vin );
5
6     input vin;
7     output voutn;
8     output vout;
9 endmodule
10
```

Fig: Verilog Netlist View

Modify the netlist so it has the following structure to provide the function required.



```
verilog.v - /home/nc3/AMI/A4407/Walkthroughs/exar
File Edit Search Preferences Shell Macro Windows
1 //Verilog HDL for "examples", "display" "functional"
2
3
4 module display ( vout, voutn, vin );
5
6     input vin;
7     output voutn;
8     output vout;
9
10
11     assign vout = vin;
12     assign voutn [= !vin;
13
14 endmodule
15
```

Fig: Modified netlist.

Now use the File -> Save and then the File -> Close options on the text window menu. Check the CIW for any errors or warnings pertaining.

9.2 Simulating and Testing the Result

We can as we have already done in Walkthrough 1 simulate and test the functionality of the verilog model to ensure that it meets our simulation criteria. As this model is integrated within the Cadence Schematic database this would be the normal approach. It is also possible to extract and simulate the model using the standalone simulation environment. It is recommended that students follow the course shown in Walkthrough 1 for reference to the route for simulation.

Full Custom Using Standard Cells

Creating a Digital Test Schematic

Use the Library browser to select the example library and the test_display_1 cell using the mouse so it is highlighted. With the mouse over the test_display_1 press the right hand side mouse button to show the context sensitive menu. Select the Copy command.

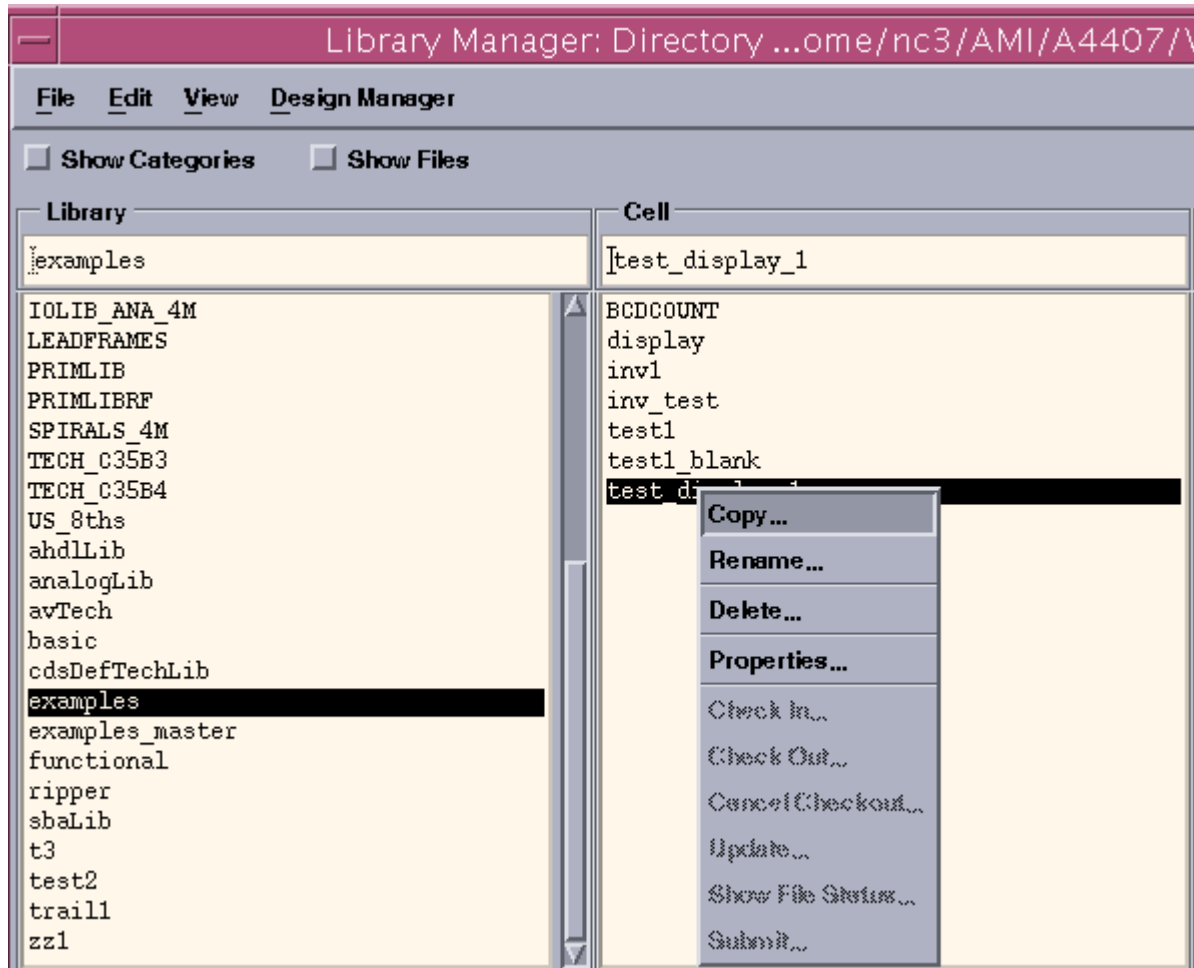


Fig: Cell Context Sensitive menu with test_display_1 selected.

Use the copy form displayed to copy this cell to a new one called test_display_2. By changing the Cell entry in the To section of the form. Then OK the form.

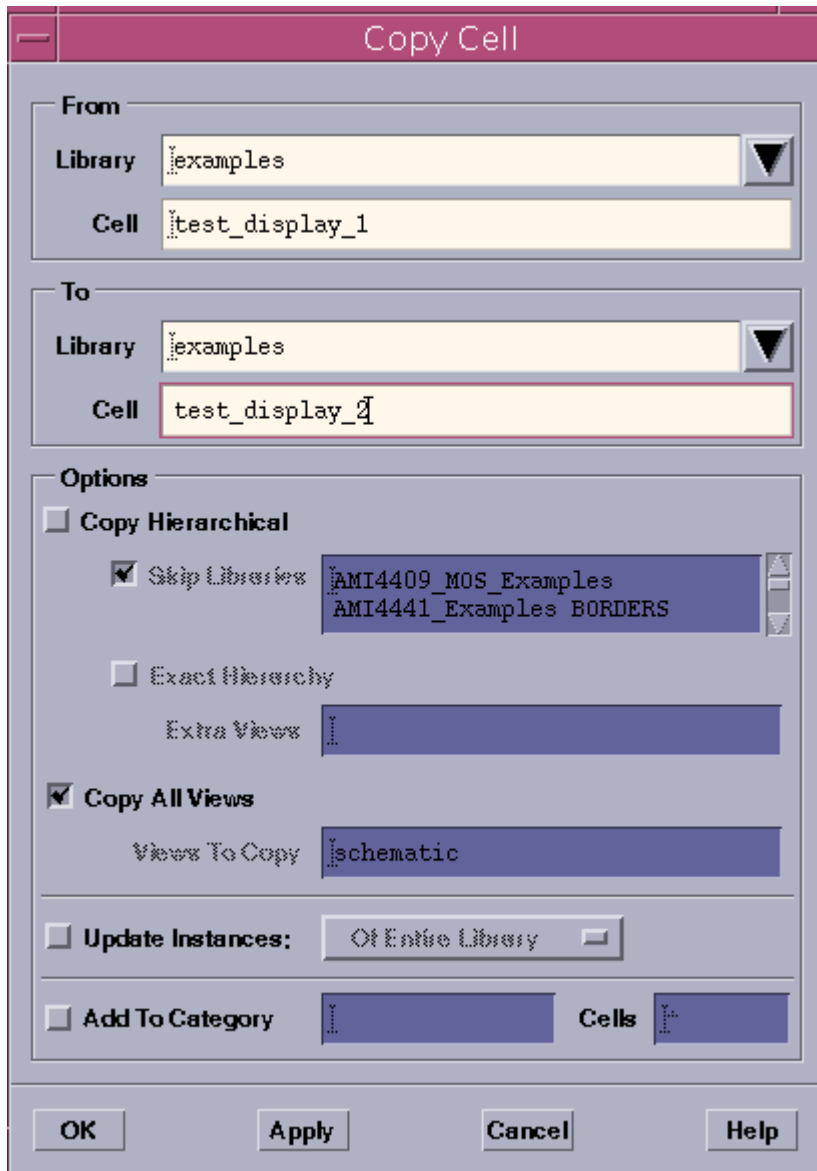


Fig: Copy from with To Cell entry updated.

Now use the library browser of the File -> Open command to open the test_display_2 schematic for editing.

Remove all the analogue components, and their associated wires from the schematic. This would be the gnd, vdd, vdc and vpulse elements.

Place a single input pin called top_vin onto the schematic and attach this to the vin input of the "display" instance on the schematic.

The final schematic should resemble the one below:

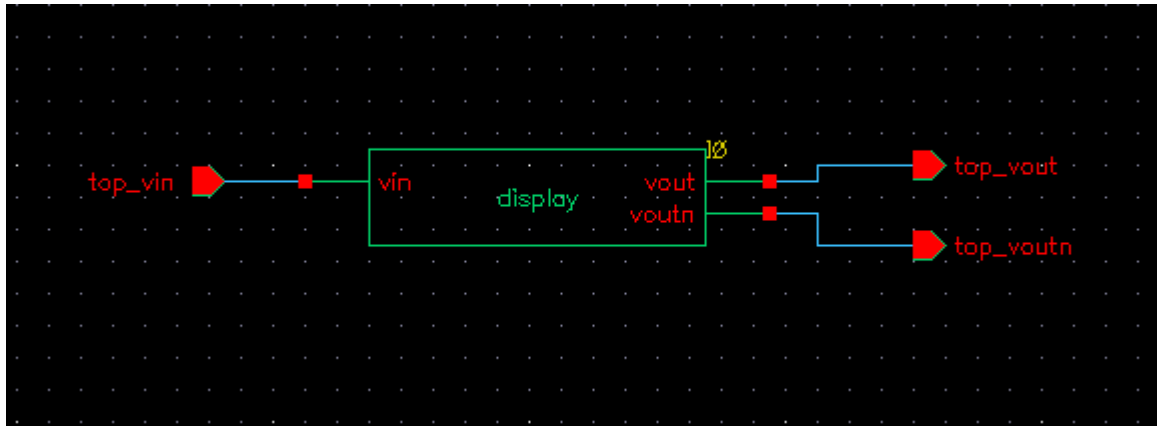


Fig: Digital Test Schematic Final Version

We can now use this test bench to run our digital simulations. As defined in Walkthrough 1.

From the Schematic use Tools -> Simulations -> NCVerilog

On the Virtuoso Verilog Environment for NC-Verilog run the following commands:

Commands -> Initialize Design

Commands -> Generate Netlist

Commands -> Edit Test fixture

On the Edit Test Fixture form "OK" the form to edit the stimulus file. In this case as it is provided here we do not need to save it.

Below the "top_vin = 1'b0" entry add the following entries

- #200 top_vin = 1'b1;
- #200 top_vin = 1'b0;
- #200 top_vin = 1'b1;
- #200 \$finish;

Full Custom Using Standard Cells

```
1]
2 // Verilog stimulus file.
3 // Please do not create a module in this file.
4
5
6 // Default verilog stimulus.
7
8 initial
9 begin
10
11     top_vin = 1'b0;
12
13     #200 top_vin     = 1'b1;
14     #200 top_vin     = 1'b0;
15     #200 top_vin     = 1'b1;
16     #200 $finish;
17 end
18
```

Fig: Final Stimulus file

Now use the Commands -> Simulate command to run the simulation. This will open up the SimVision Windows. Use the Design Browser to select the signals, (Click on the test in the LHS pane and then right click to display the context sensitive menu and select "Sent to Waveform Window" or use the icon as per Walkthrough 1.

Once the waveforms are displayed in the Waveform window. Select the Simulation -> Run option from one of the simvision windows.

Return to the Waveform Simvision window and do a View -> Zoom -> Full X command to display the entire simulation. The result should resemble the one below.

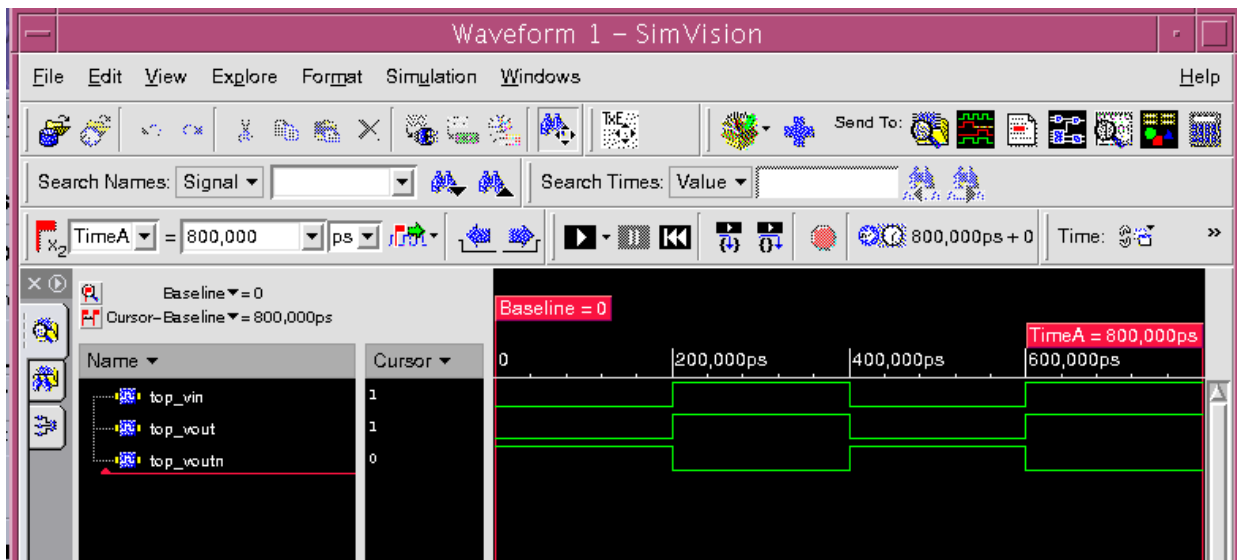


Fig: Successful Simulation after View -> Zoom -> Full X

10 Summary

You have now successfully simulated the analogue and digital versions of the schematics.

Make sure you save all data and then close the relevant windows.

11 Layout

Analogue Synthesis is another of those currently impossible items on the list. Whilst digital synthesis, along with automatic place and route have been providing the ability to place millions of gates on chips in an efficient manner analogue synthesis is still not a viable route to the production of a layout. Ignoring the complexity of issues that impact analogue design, the increasing difficulties engendered by DSM issues. Analogue design and layout still remain the remit of the experienced engineer. Familiar with the process and the requirements of the structures. The following is a very brief example of why automated analogue synthesis is not a mainstream product.

A number of the tools that could be used have no rules decks provided for the AMS 0.35um technology. The complexity of these tools at the moment limits the amount of functionality that can be built in the time available. Hence we will use a limited subset of the tools available.

Covering even basic issues of common design habits, the design rules for a process, the DRC, ERC Power, Antenna and LVS rules and checkers as well as the routing tools, each one of which could quite usefully fill many modules is a problem.

Students will not be expected or required to produce any form of custom layout and are recommended to read Dan Kleins excellent primer on basic layout.

However for those who wish the experience this is the basic route to be followed for the AMS 0.35um technology.

11.1 Introduction

This section will take an existing schematic, “synthesize”, automatically place and then route the cell. It will then run a DRC on the design.

11.2 Creating the Basic Layout From the Schematic

Open up the schematic, library example cell name display, using either the File -> open or the library browser. From the schematic menu select the command: Tools -> Design Synthesis --> Layout XL. This will open up a basic form, asking if you want to create a new design or open an existing one. In this case use the default of “Create New” and OK the form. This will open the “Create New File” OK this one as well. This will create the layout view. It will also open up the LSW layer file.

- Tools -> Synthesis -> Verilog XL
- Create New Form “OK”
- Create New File Form “OK”

Full Custom Using Standard Cells

- On the Virtuoso XL Layout Editing view select the Design -> Gen from source command. OK the form.
- As you can see the transfer is aware of the pins and power connections required and has assigned them a default metal layer and size. All of which is configured in the tech file. Again we are going to use the defaults as much as possible for this exercise.
- Design -> Gen From Source
- Layout Generation Options form OK

The layout should now resemble the one shown below:

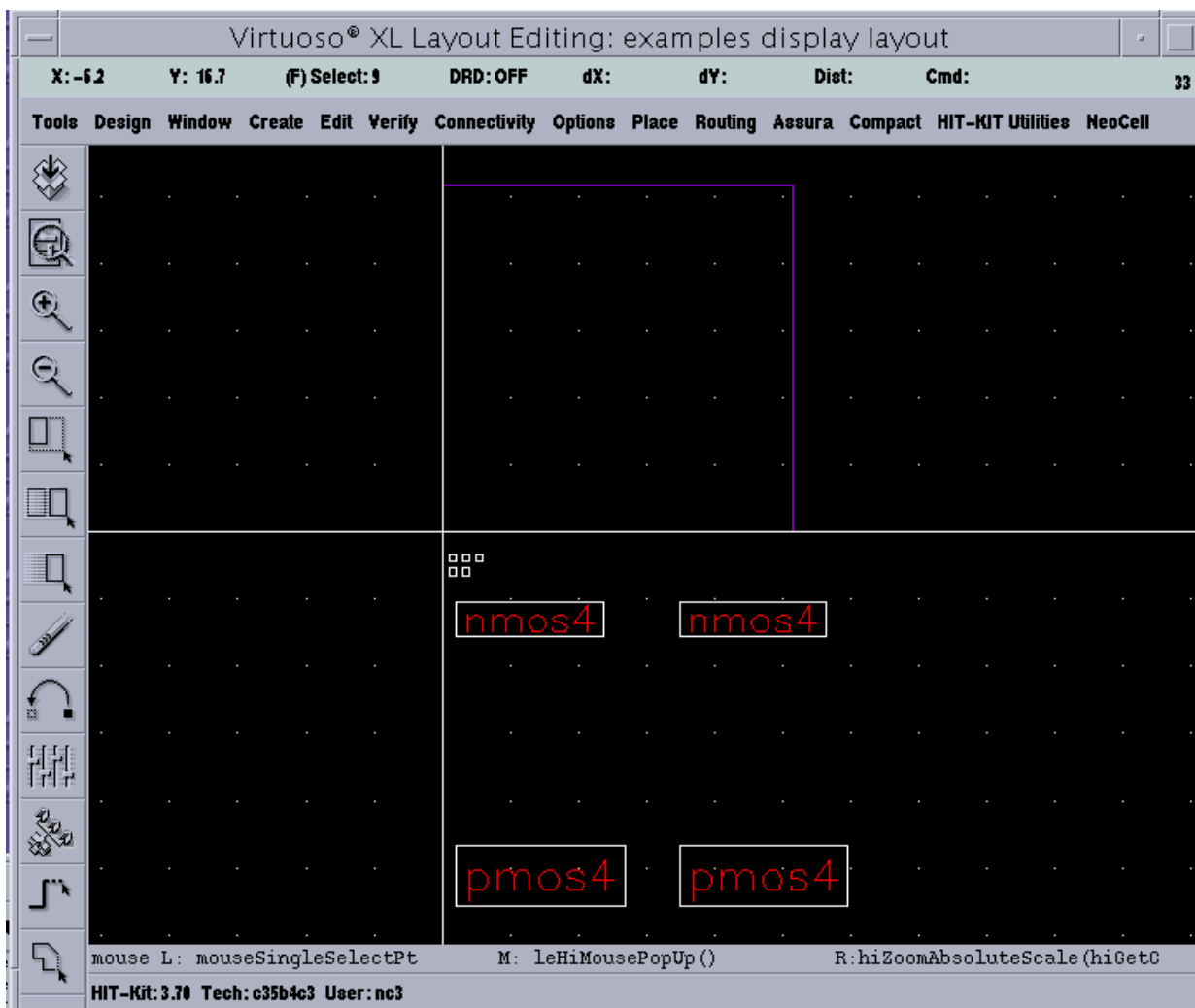


Fig: Pre Placement Layout

To automatically place these components use the command Edit -> Place as in Schematic. OK the form that is displayed

- Edit -> Place As In Schematic
- OK Form

The final result should resemble:

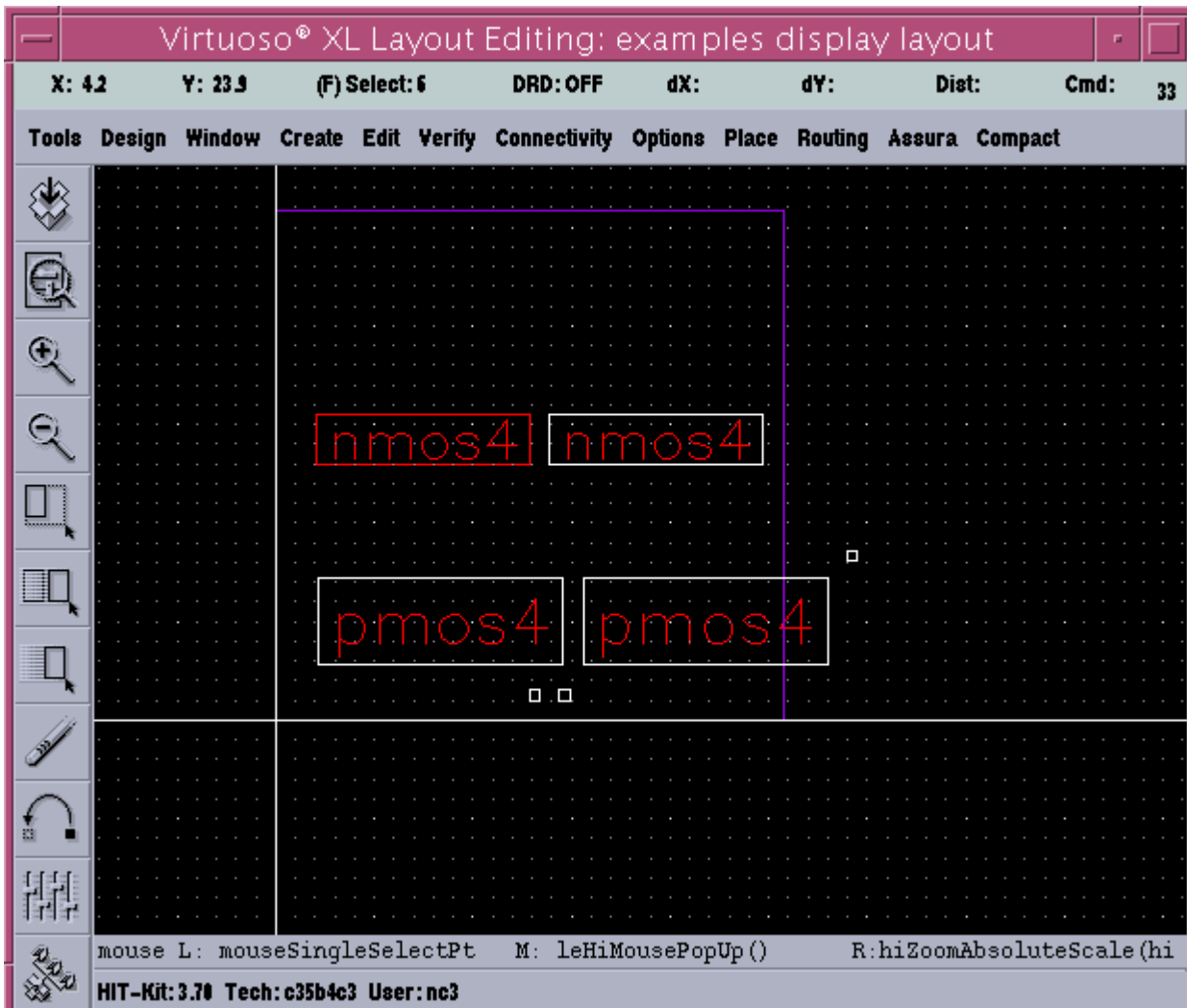


Fig: Post Place As In Schematic

11.3 Things we need to do

In order for the router to work all the devices must be inside the purple box. So left click to select and then drag the block to place it inside the purple block. Which the autoplacement has not done.

Turn on flight lines so we can see the connections.

Connectivity -> Show Incomplete Nets will display the Show Incomplete Nets form. Use the "Select All" option on the right side of the incomplete nets to transfer all nets. Then "OK" the form.

- Connectivity -> Show Incomplete Nets

- Show Incomplete Nets Form “Select All”
-

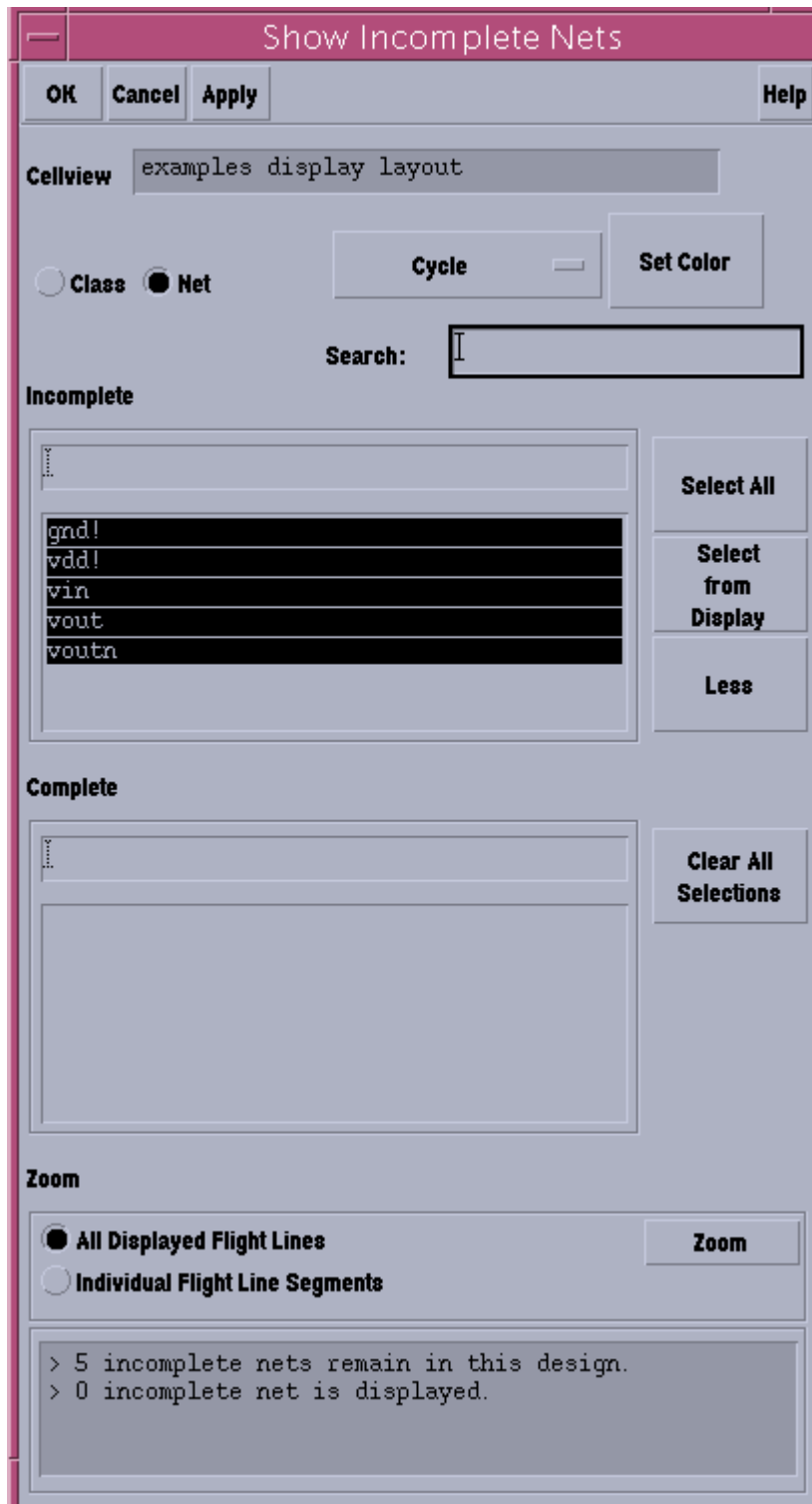


Fig: Show Incomplete Nets Form after Select All

The layout will now change to show the required connectivity and relationships.

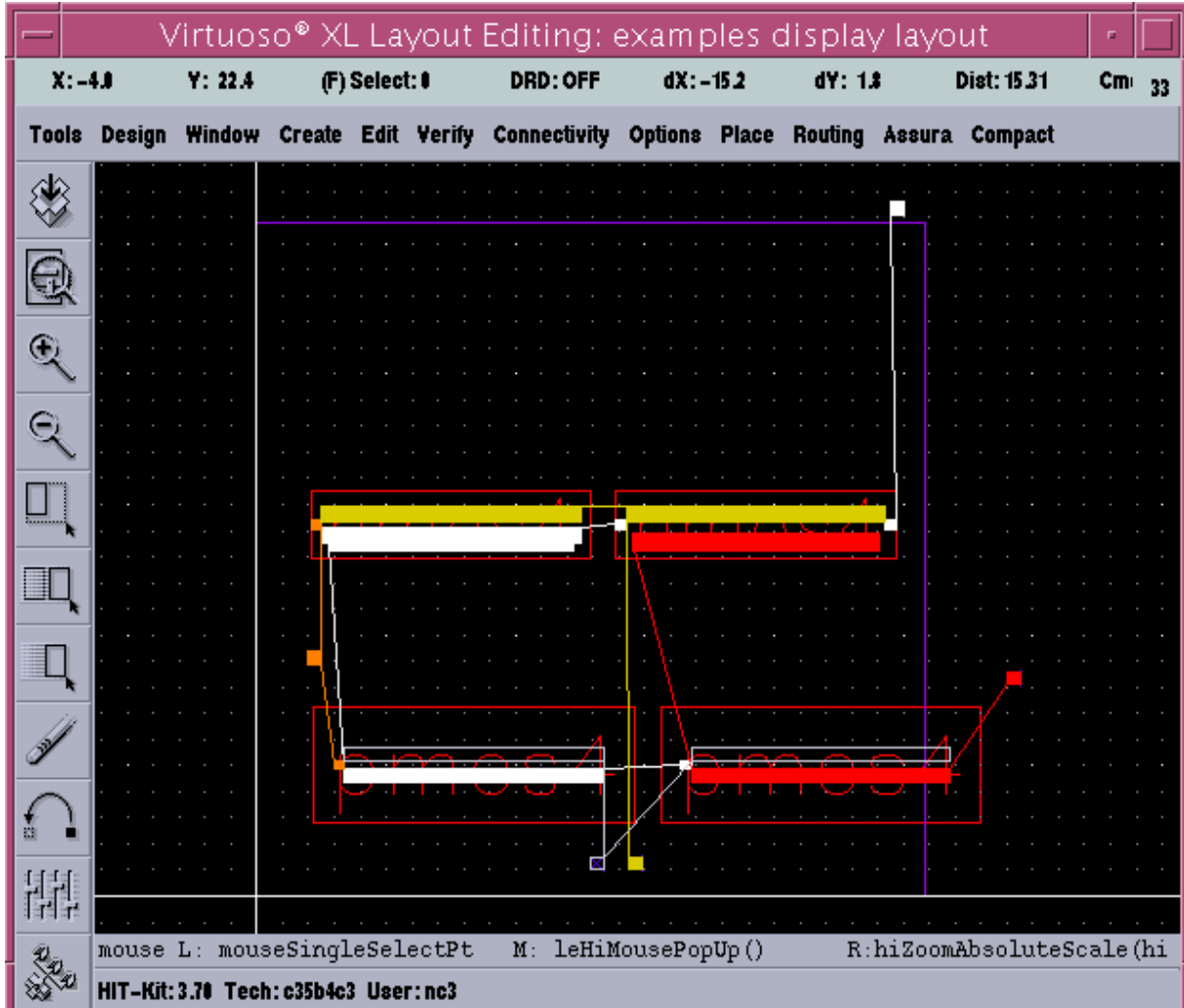


Fig: Layout Showing all incomplete Nets

11.3.1 Routing

We need all the objects, including pins inside the place and route boundary (purple box). To do this we need to select them with a left mouse click, or draw a box around them with the left hand mouse button held down. We then need to use the Edit -> Move, bind m or the icon to select move. By default move is orthogonal. You only get to move things in one plane for each move i.e. only X or only Y. Use the F3 button to invoke the move options form and change the snap from orthogonal to any angle.

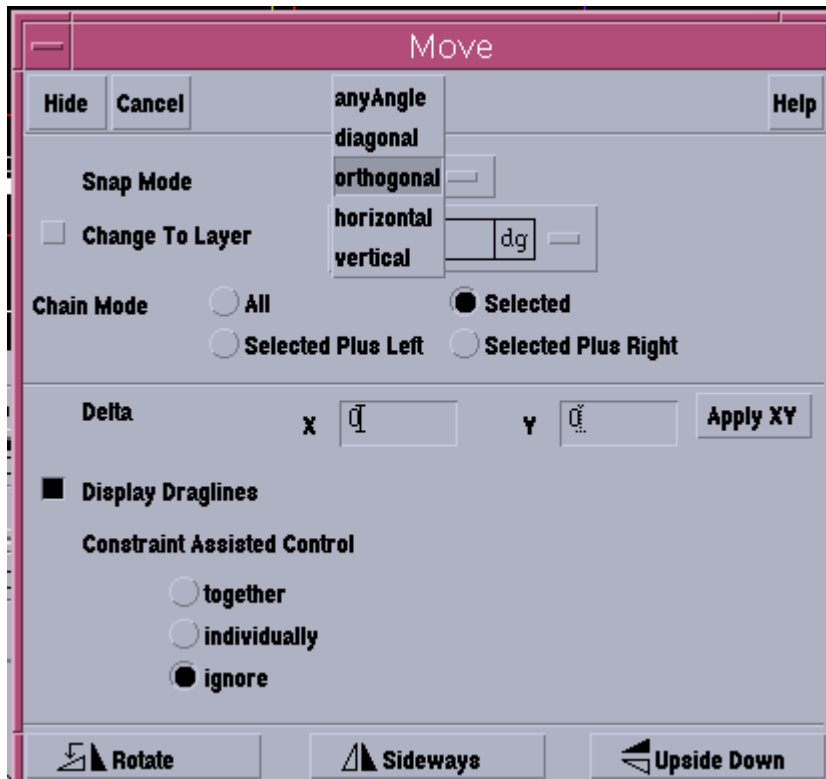


Fig: Move Form with Snap Mode Selection

Move all items within the purple box. Including the pins.

Hint: selecting an area is often easier to locate and move a pin.

11.4 Routing the design

Once all the items are within the bounding box we can use the autoroute. Let me assure you that for this sort of design manual placement and routing would be the order of the day. I have left the design somewhat spaced out so the routing can be seen.

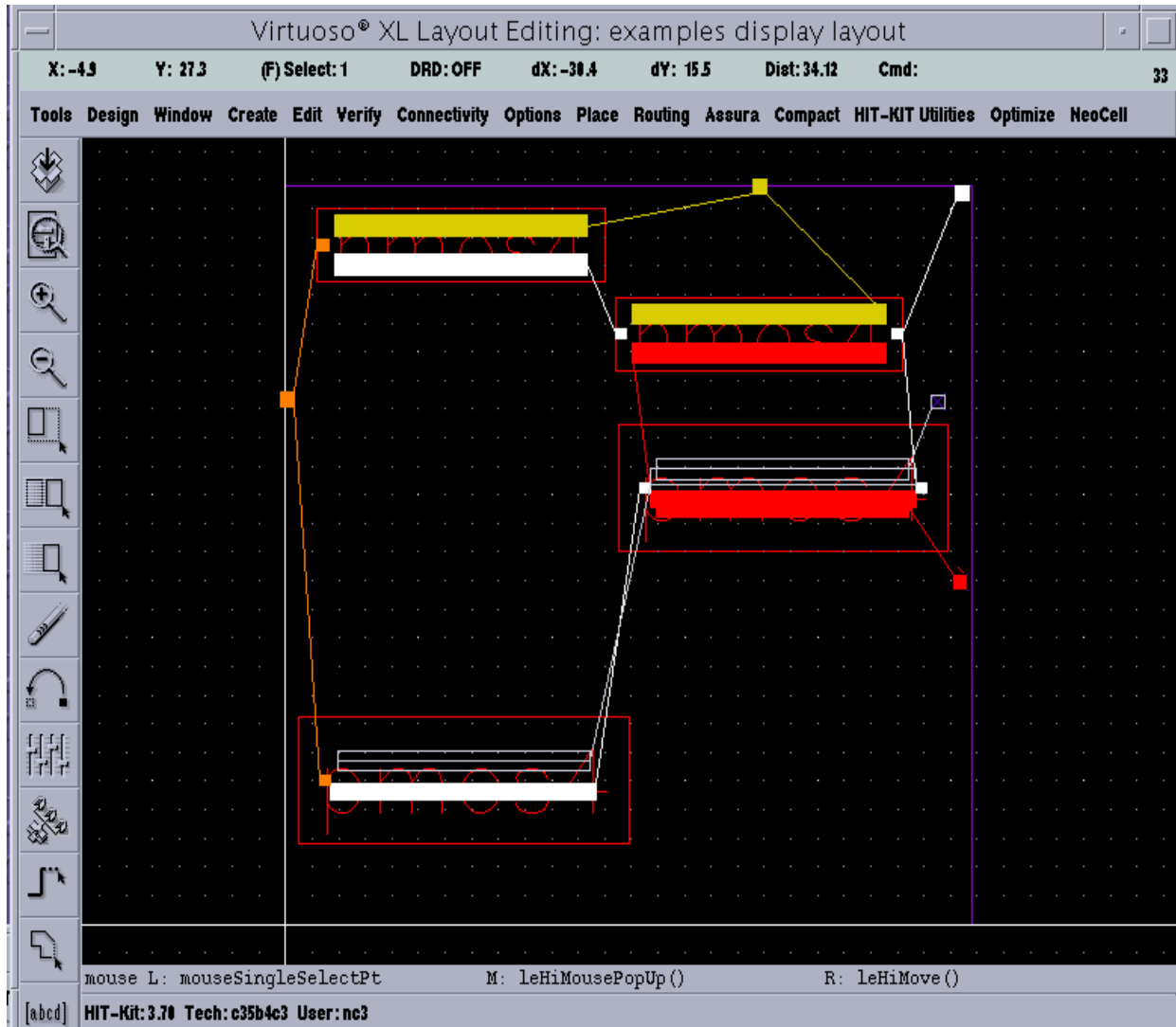


Fig: Pre Placement Design

Select the Routing -> Connect to Router Option.

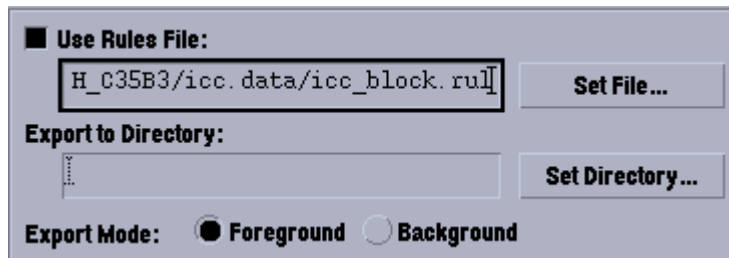
Use Rules File entry and using the Set File option set the following path:

- /cad/DesignKits/Europractice/AMS/ams_v3.60/artist/HK_C35/TECH_C35B3/icc.data/icc_device.rul

Make sure you select the icc_device.rul and not the icc_block.rul!

That section of the long from should resemble:

Full Custom Using Standard Cells



Export To Router Rules Section

Hint: The set file form is a tad strange, you may need to use the Arrows on the left hand side to move up and down the hierarchy.

OK the form the will invoke the Router, in this case the Virtuosos Chip Assembly Router. It should resemble this:

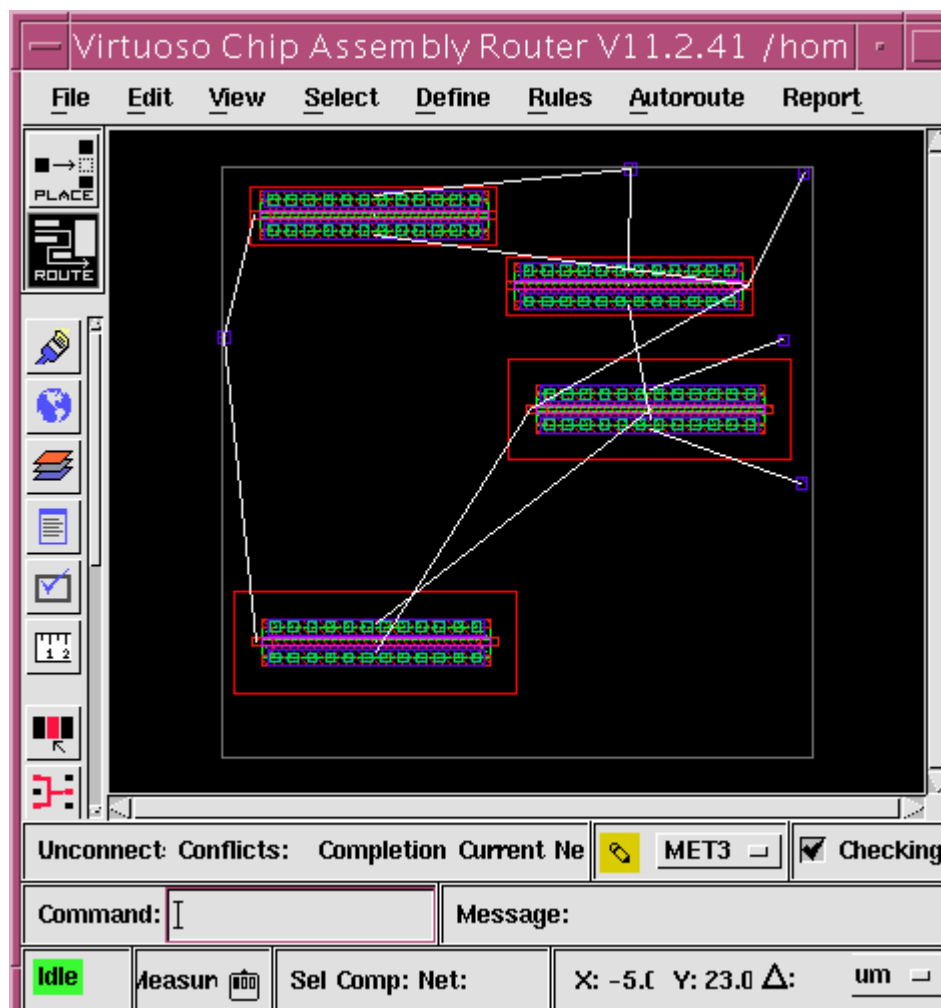


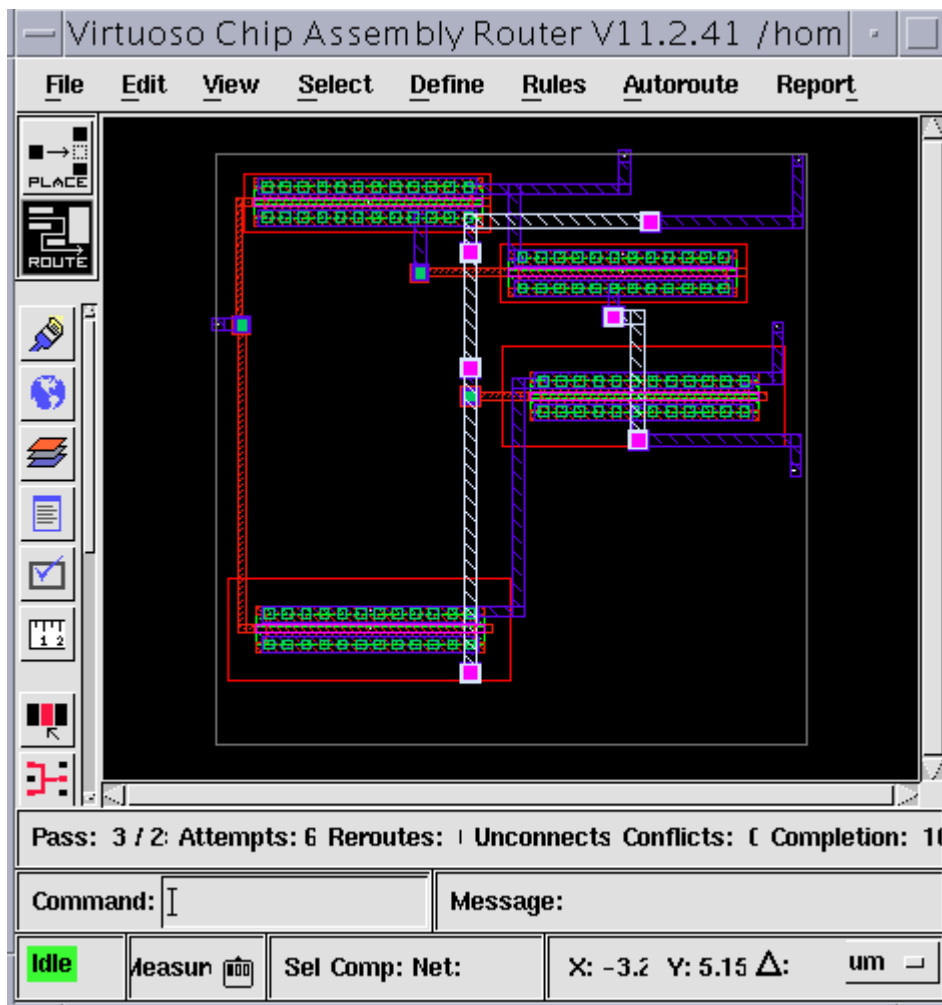
Fig: Virtuoso Chip Assembly Router Pre Routing

Full Custom Using Standard Cells

As we are doing a device placement the display has changed to display all layers as you can see by the complexity of the elements.

At this level we can move directly to final routing. So we can use the Autoroute -> Detail Route -> Detail Router menu option to generate a route. OK the Autoroute form and the structure will be routed.

- Autoroute -> Detail Rout -> Detail Router
- OK AutoRoute Form
- The final result for me is shown below.
- As you can see the router used:
- Metal 1 Purple
- Metal 2 White
- Via1 Pink
- Poly1 Red
- Contacts Green



Full Custom Using Standard Cells

In part because elements deliberately setup the layout so it would have to route through and around elements.

Cleaning

Now run the Autoroute -> Clean command. This will endeavour to “tidy” up the layout. It is more effective, and takes a lot longer to run on larger designs.

Transferring this back to the layout.

Close the router. You will be prompted to save the ses file. Execute a “Save and Quit” but make a note of the path to the file. In my case it was “.displayc17427/display.ses”. Any other prompts just answer yes/ok to.

In the Virtuoso Layout XL Editing window use the Routing -> Import From Router Command. You should find that the “Import Router File” is already set. “OK” this form.

- Routing -> Import From Router
- Import From Router Form “OK”

This will update the routing on the layout.

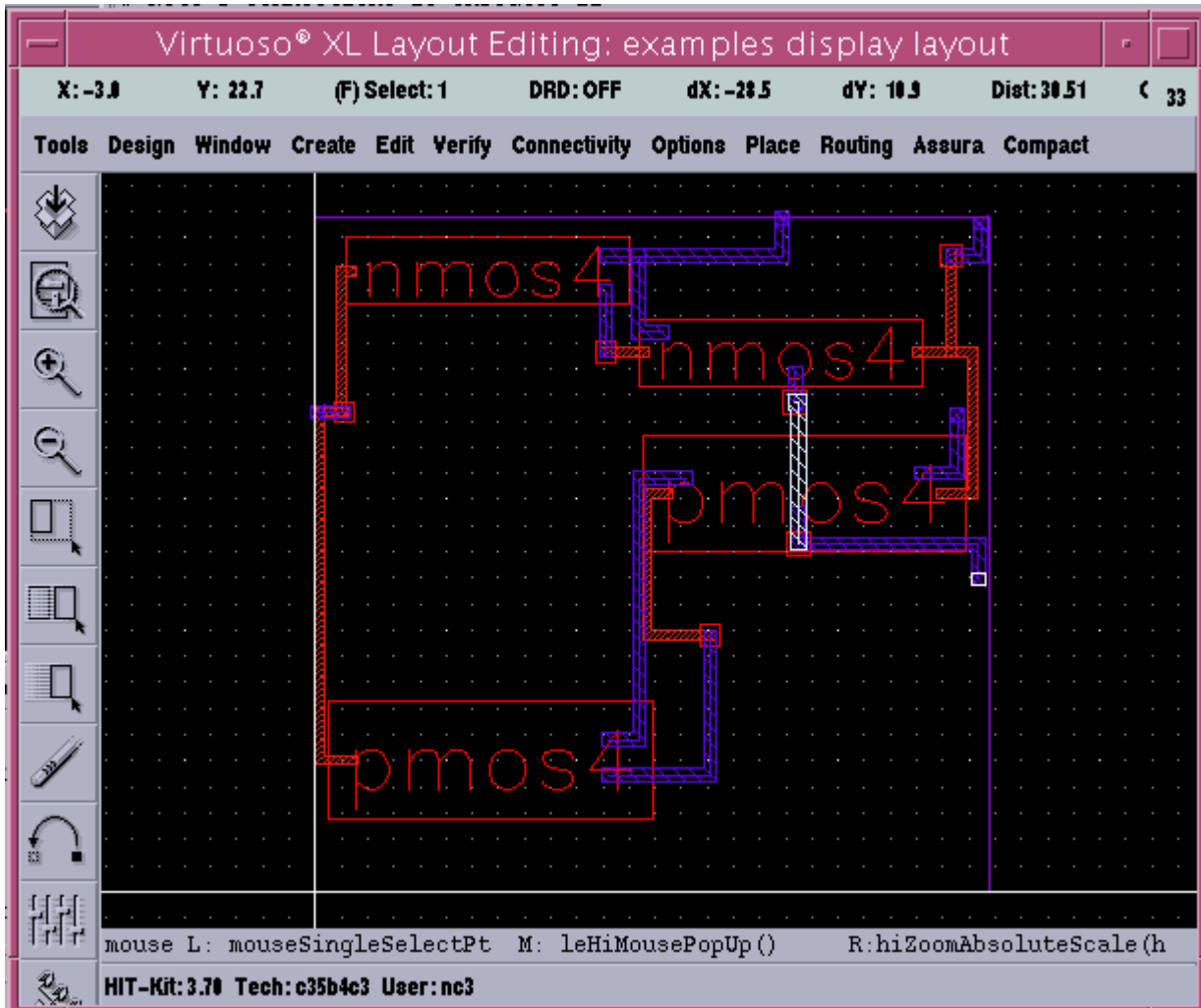


Fig: Final Layout Version

To see all the complexity use the Options -> Display to display the display form and change the stop level to 20. This will display all the layers visible. To go back to the block view change it to 0 again.

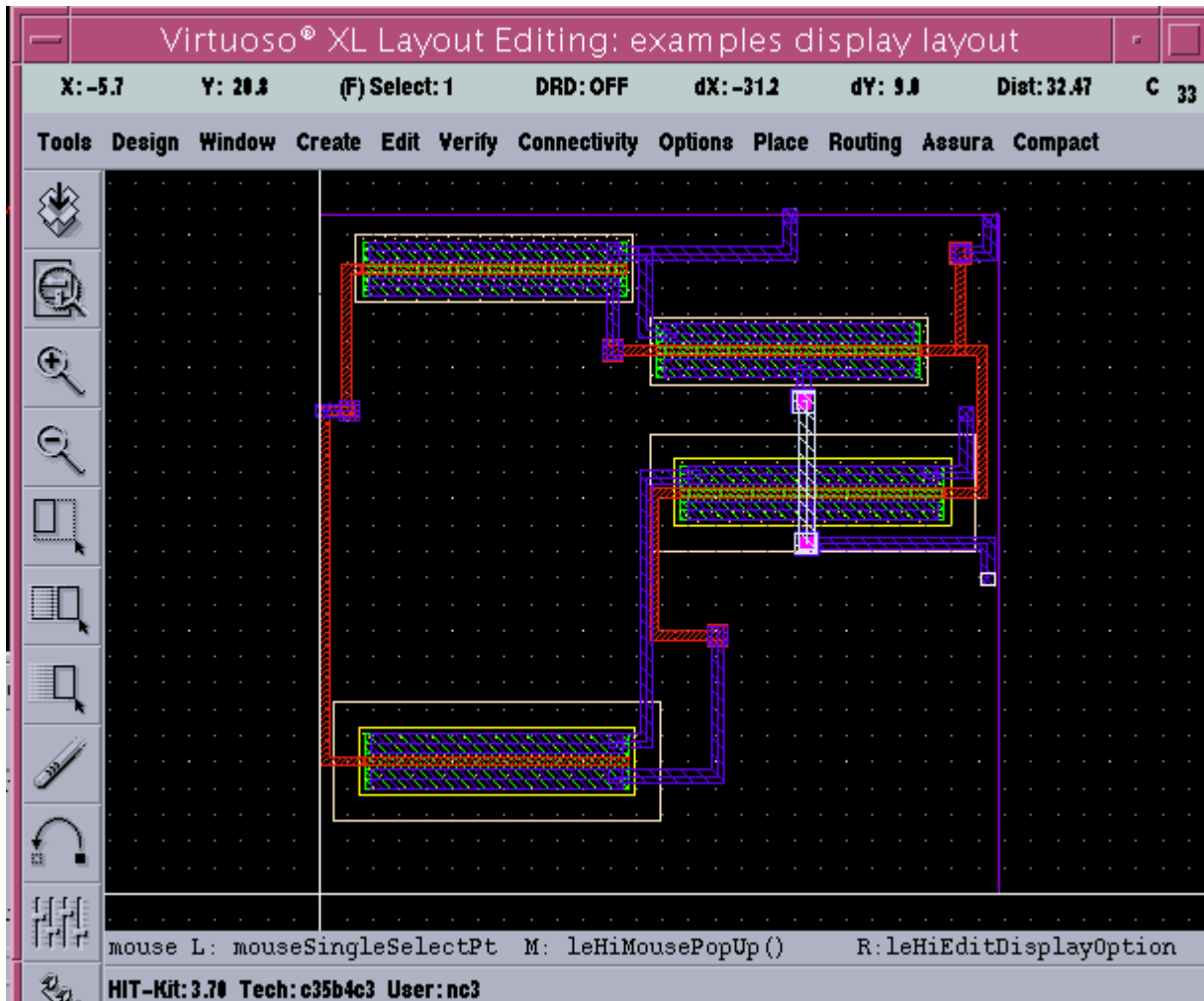


Fig: All Layers version

Running a DRC

Select the Assura -> DRC option. When the form is displayed OK this form. When the run is finished you will be asked if you wish to display the results. They will show a considerable number of DRC issues. One reason why we are using standard cell design is the actual complexity of actions required to produce a clean DRC under these circumstances.

Below is a "standard" comprising of two inverters i.e. a buffer cell that passes all DRC requirements. This is equivalent to our design. Compare the overall structure and packing. As it is a standard cell one technique that is not commonly used i.e. diagonals has been used.

