Current-carrying capacity

1 Some historical background

The charts currently in IPC-2221 Figure 6-4 are evidently of ancient origin, but, at the time the document was produced, IPC did not know where the charts originated. It was thought that they were based on studies by Dr. Jennings at Sandia Labs in New Mexico, for IPC-TP-117. This work had been formalized in MIL-STD-275, and subsequently in IPC-D-275, a replacement document created after the Perry Initiative[1].

The use of these charts in the way described in the standard is not ideal, as it is difficult to do, prone to error, and yields imprecise results. In consequence, a number of efforts have been made to translate this information into a mathematical model. As an example of this, UltraCad Design's website has a calculator made by Doug Brooks that is based on IPC-D-275. His modelling approach is discussed at http://www.ultracad.com/pcbtemp.pdf. Other equations for IPC charts come from a technical paper by McHardy and Ghandi. Minor differences between such models and the standards originate in differences in the curve-fitting techniques used to represent the charts.

Believing the models to be inaccurate, current-carrying capacity studies were initiated by work on the satellite project Stardust. After 14 years of doing thermal analysis, electrical engineers were, for the first time, able to model the power dissipation of internal traces in a circuit card.

An early application of this work was in advising on a crucial reliability-related issue. A satellite had gone through qualification testing and someone had accidentally applied 8.57A to a trace. According to the IPC charts, even assuming the less stringent model where the trace is on the outside of the board, the trace would have been at severe risk of failure, so that the only prudent action would have been to examine/replace the board at huge cost.

In the event, the analysis showed that the thermal excursion, though severe, was well within the capacity of the board. Critically, there was little relation between observation/model and the IPC charts.

This was one of the drivers that spurred Mike Jouppi (now of Coretec) to investigate both the charts and the source of the data used to create them. He found that:

- All the charts could be traced back to a very early report commissioned by the Navy Bureau of Ships: NBS (National Bureau of Standards) Report #4283 *Characterization of metal-insulator laminates*, D.S. Hoynes, May 1, 1956
- In Hoynes' report, the original Design Chart is clearly marked 'tentative'

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[1] On 29 June 1994, US Secretary of Defense Perry signed his policy *Specifications and Standards – a new way of doing business* which dramatically changed the way requirements would be written in acquisitions. The policy directed the use of performance and commercial specifications and discouraged the use of military specifications and standards by requiring the approval of a waiver. This DoD policy was fully implemented by the end of 1994.

- The work was carried out on the external layers of double-sided material. Whilst this was state-of-the-art at the time, it is hardly representative of modern constructions
- At the time of the MIL-STD-275 conversion, charts for internal layers had been created by the simple, but arbitrary and unvalidated, expedient of derating those for external layers by 50%.

In summary, IPC 2221, IPC-D-275, MIL-STD-275 are all copies of the conclusions of the NBS study, are based on inadequate and historic information and, for internal tracks, are empirical rather than supported by test data.

2 Facts, not guesswork

Mike Jouppi of Coretec, the instigator of the investigation, and a researcher in the field since 1998, is now chairman of the Task Group preparing a new IPC Standard, IPC-2152, *Standard for Determining Current Carrying Capacity in Printed Board Design*, which was initiated at IPC Expo 2002, and is scheduled for release in 2003. It is Mike's compilation of literature research, testing and analysis that forms the basis of this document.

The analysis starts with the observation:

Conductor width, thickness and length drive the resistance. The resistance and current drive the power dissipation.

However, the relationship between heat dissipation and the resultant temperature rise needs to be quantified. Jouppi makes the point that "there is more to sizing conductors than just current, cross-sectional area and temperature rise", although these remain the main drivers. Some of these influencing factors are:

- substrate thickness
- substrate material
- the presence of copper planes
- the environment (vacuum; air; forced convection)
- the power dissipation
- mounting configurations and orientation

There are also time dependencies. As with any situation where a physical body is heated, there is a rise and fall time associated with the thermal mass of the structure and its relation to the heat available and the cooling mechanisms. Current switching may be instantaneous; its thermal results have much slower edges.

Jouppi set about measuring the actual rise in temperature, and investigating the incidence of some of these factors. His test method was based on IPC-TM-650, Method 2.5.4.1, and his test vehicle is shown diagrammatically in Figure 1. Data was collected on six different trace widths from 127 µm to 2.54 mm, using both 2 oz and 3 oz external copper and ½, 1, 2 and 3 oz internal copper.

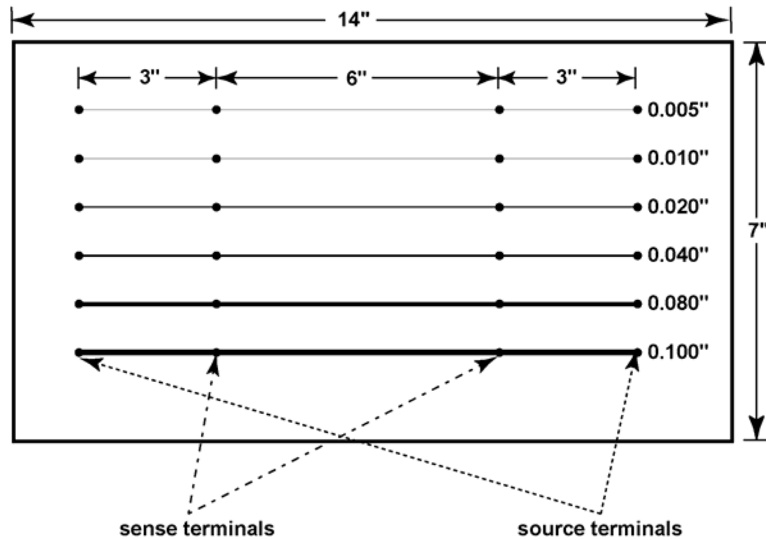

Figure 1: The test vehicle

The test used was based on Method 2.5.4.1 – if you are not familiar with this, then you should download it from www.ipc.org/download. The basis of the method is to measure the average temperature of the trace by its effect on the resistance of the track, copper having a positive temperature coefficient of resistance (TCR) of around 3,930 ppm/°C. Needless to say, the measurements are four-terminal, to allow for the low resistance value, and the TCR is measured rather than assumed.

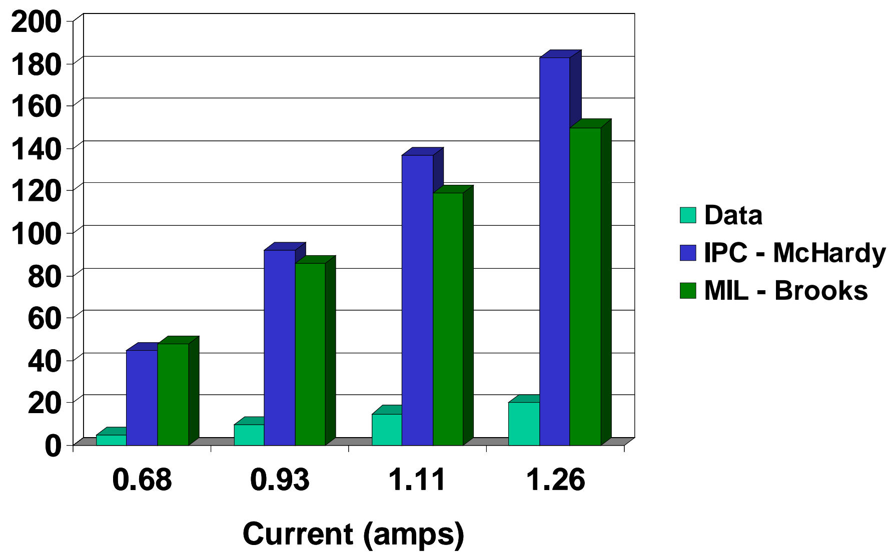

Figure 2: Comparing theoretical and actual temperature rises

Figure 2 compares theoretical figures for a 10 sq. mils internal trace in 2 oz copper on 70 mil polyimide against actual measured data. Both the IPC figures and those calculated from the Brooks model, although relatively close to each other, are well above the actual temperature rises experienced.

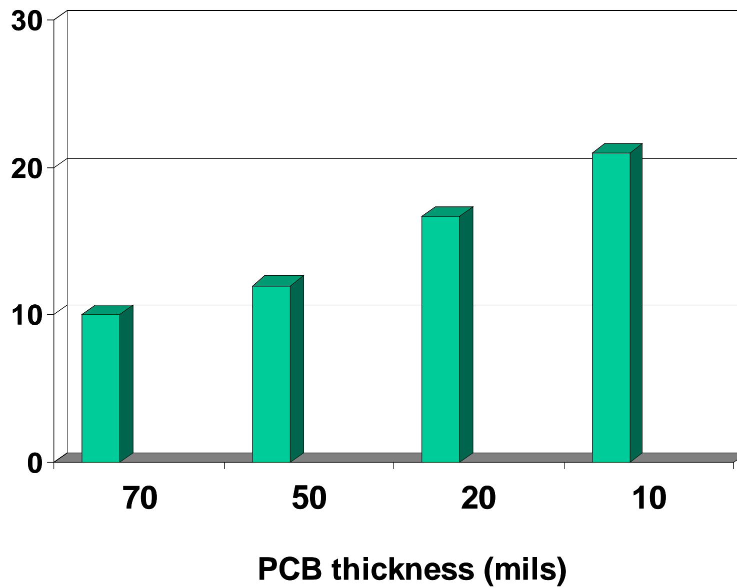

Figure 3: The effect of substrate thickness

Figure 3 shows the effect of substrate thickness for the same trace width, copper thickness and current, but with the polyimide substrate thickness reduced progressively from 70 to 10 mils. As you will see, the effect is far from negligible, suggesting that one reason for the high values predicted by IPC is the poor conductivity of initial sample substrates.

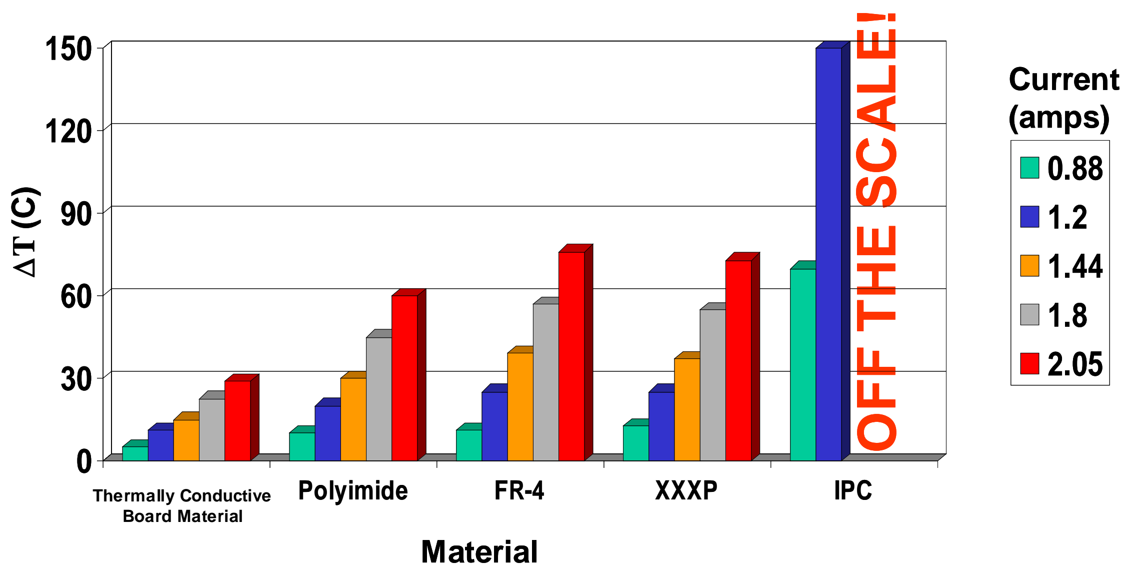

Figure 4: The effect of changing substrate material

In Figure 4, we see the effect of using substrate materials other than polyimide. The materials with phenolic and epoxy resins are less good conductors than polyimide, and a considerable improvement is made by formulating the resin with thermally conductive additives – the reduction is around 60%. Note that for all these materials, the projections of the IPC model are off the scale!

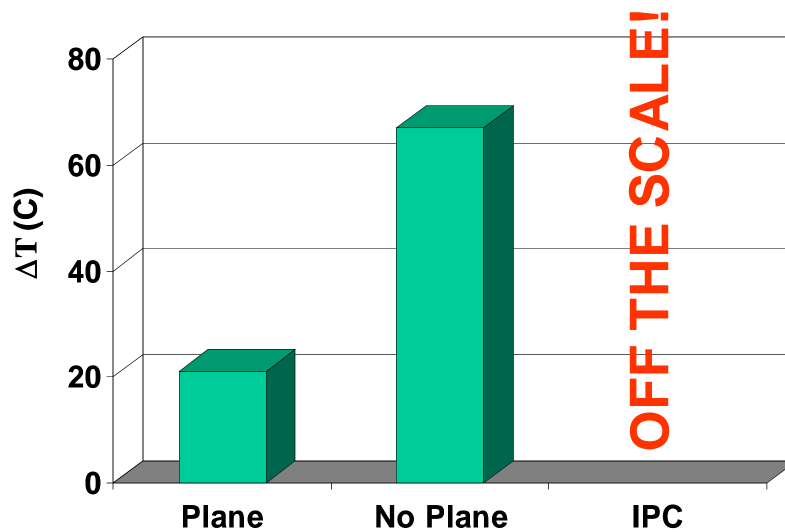

Figure 5: The effect of adding a copper plane

Figure 5 shows the effect of adding a copper plane. In this case the trace was in 3.22 sq. mils in 1 oz copper, with a 2 oz copper plane 5 mils behind the trace. A 1 A current generates over 60°C temperature rise in a vacuum, as against less than a third of that when the plane is present.

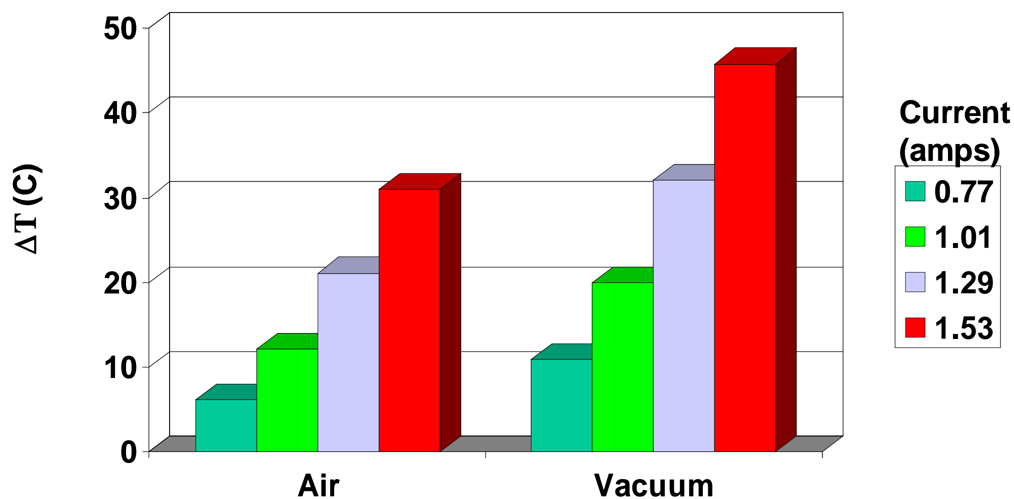

Figure 6: The effect of the environment

As can be seen by comparing Figure 5 and Figure 6, the effect of adding a copper plane is considerably more than the effect of going from a trace in vacuum to a trace in air. In other words, the contribution of thermal conduction through the board is greater than losses due to convection.

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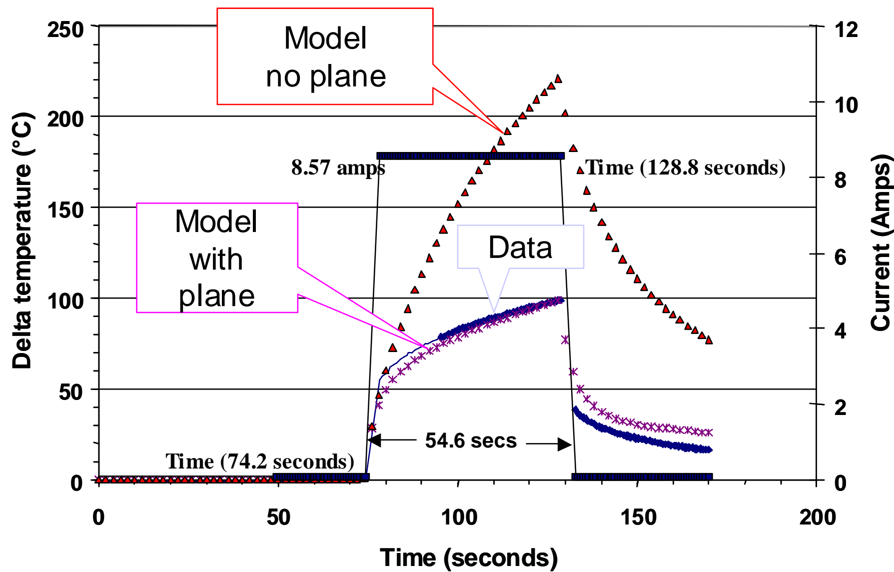

Figure 7: Transient response

Figure 7 shows the time dependency of a 0.5 mm wide internal trace made of 1 oz material. This replicates the fault situation on the satellite board. As can be seen, the pulse was applied for less than a minute and the rise in temperature observed. With no plane, the model shows a very significant temperature rise within the time of the pulse, certainly to the point where the adhesion between trace and board would have been compromised. However, given the close proximity of an internal plane, both measured data and model show a temperature that has been contained to under 100°C. Although not shown on this diagram, 100°C rise is predicted by the IPC charts for that size of trace for a current only just above 4 A: on the I^2R principle, we should have had meltdown!

3 Creating the model

The new model that Jouppi built relates conductor heating to the power dissipated in the trace. The data on which the model was based was measured by applying an stepwise-increasing current to the trace, and measuring the corresponding temperature rise. The experiments were carried out over an extended time, because the current was only increased after the track had reached a steady state temperature.

Figure 8 shows the plots of current and temperature rise for a 10 sq. mil conductor in a 2 oz thick internal layer using a polyimide laminate. The current applied to the track is shown on the secondary Y-axis on the right; on the left is the rise in temperature, shown as a smooth line joining the points. The model is the series of squares – note how close the model is to the data.

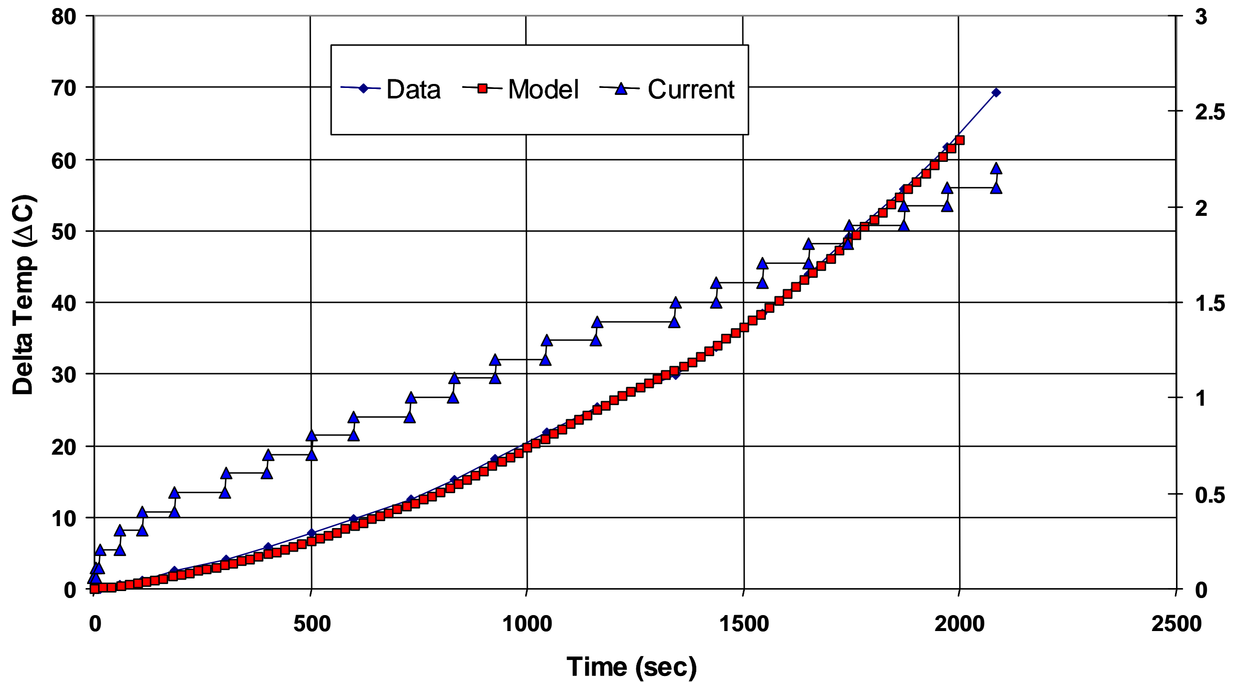

Figure 8: Collecting data for the model

The model also used accurate values for copper resistivity in the equation for track resistance:

$$R = \rho_V \cdot \frac{L}{A}$$

where R = resistance
ρ_V = volume resistivity
L = length of the conductor
A = conductor cross-sectional area

Jouppi found that the resistivity was *higher* for ½ oz copper than for copper of 1 oz or greater weight. The figures tie in well with actual measurements, but investigation is ongoing on the appropriate values for thinner and heavier copper.

The model also allows for the fact that:

- resistance will change with trace temperature
- resistance will increase with applied current
- resistance will increase due to board heating

It is easy to forget that the TCR of copper is very significant, being almost 0.4%/°C.
By contrast, most chip resistors have TCRs of only 100 ppm (0.01%/°C), so we can generally ignore temperature changes – that is *not* the case here!

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4 Modelling the effects

Given that the conceptual model for heating produced a good match to the data for isolated tracks, Jouppi was able to extend this to evaluate other design features by using finite element modelling methods.

IPC states that conductors can be **necked down**, in order to provide sufficient clearance to adjacent lands, but does not provide any means of estimating the effect that this will have on dissipation. Take the case of a 5 mil conductor that is necked down to 2 mil. The IPC chart indicates a maximum current of 0.27 A; new test data indicates that this figure should be 0.76 A. Moreover, the Jouppi model predicts the power dissipation for a 5 mil trace for a 10°C rise at an ambient of 25°C as 131 mW, and for a track including the neck-down only marginally higher at 145 mW.

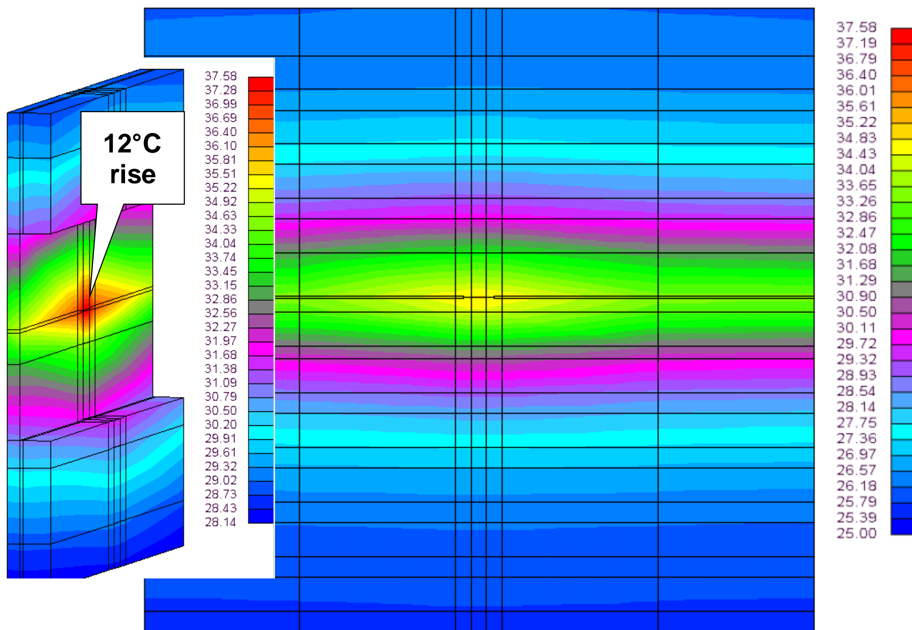

Figure 9: Temperature rise for a necked-down trace

On the left of Figure 9 is a view of the trace with a section of the model cut away; on the right is a front view of the model showing the temperature distribution on the exterior face of the card – the temperature rise shown is only12°C.

Similarly, the model can be used to show the effects of an **internal copper plane**. Figure 10 shows the same necked-down trace, but with a full ground plane The temperature rise is more than halved to only 5.5°C.

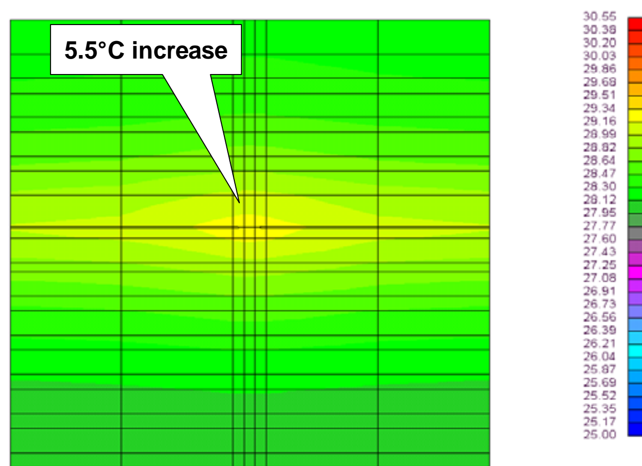

Figure 10: Temperature rise for a necked-down trace with ground plane

Contrary to expectations, cut-outs in the plane seems to have little impact. Figure 11 shows one level of cut-out, for which the temperature rise is very similar to that for a full ground plane.

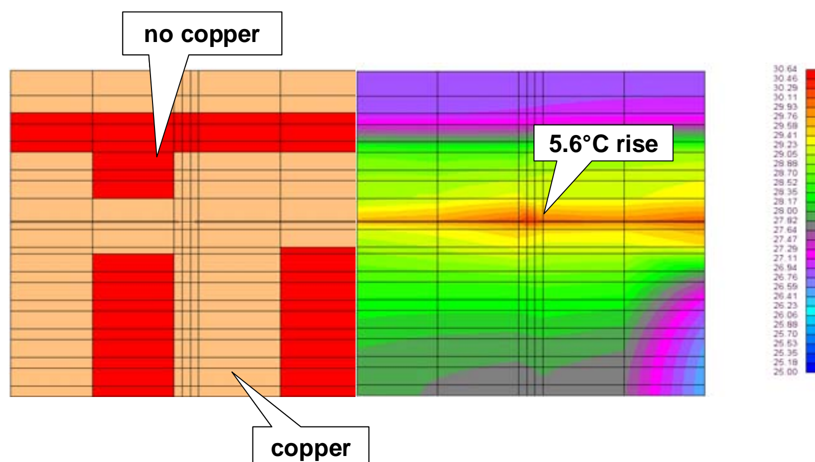

Figure 11: Temperature rise with cut-outs in ground plane

When removing further copper (Figure 12), one can begin to see a difference, but still the shape of the temperature profile shows how the copper helps spread the heat. Removing copper in the area of the neck-down of the trace is what creates the greatest temperature rise.

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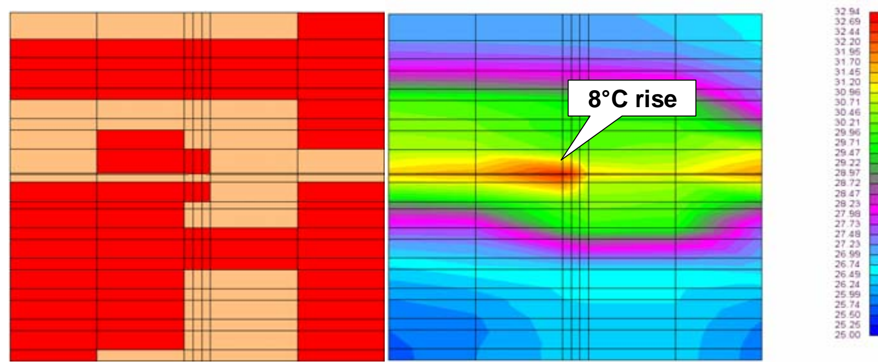

Figure 12: Temperature rise with more cut-outs in ground plane

Remarkably, even with a very small area of copper in the internal plane (Figure 13), there is still a small improvement in the track temperature. The inference is that, in a multilayer board, the combined effect of the copper layers will do much to spread the heat dissipated in the track.

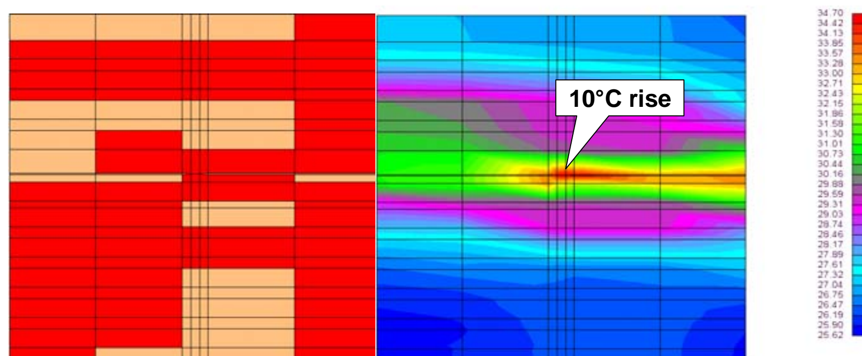

Figure 13: Temperature rise for minimal ground plane

5 Further work

The need for a more sophisticated model than the original IPC-2221 is quite clear: one has to understand all the drivers affecting track temperature rise, and not just the ohmic heating in the track. Certainly knowing the facts helps to provide solutions that are not possible within existing design rules. The new Standard IPC-2152 will go much of the way towards using more realistic estimates of heating.

However, this is not the end of Mike Jouppi's work, as his research continues with different weights of copper, different test methods and the effect of different laminate materials, seeking to build up a thermal model database.

Acknowledgement

The course team are grateful to Paul Cooke of Coretec (http://www.coretec-inc.com/) for making Mike Jouppi's source material available for this note.